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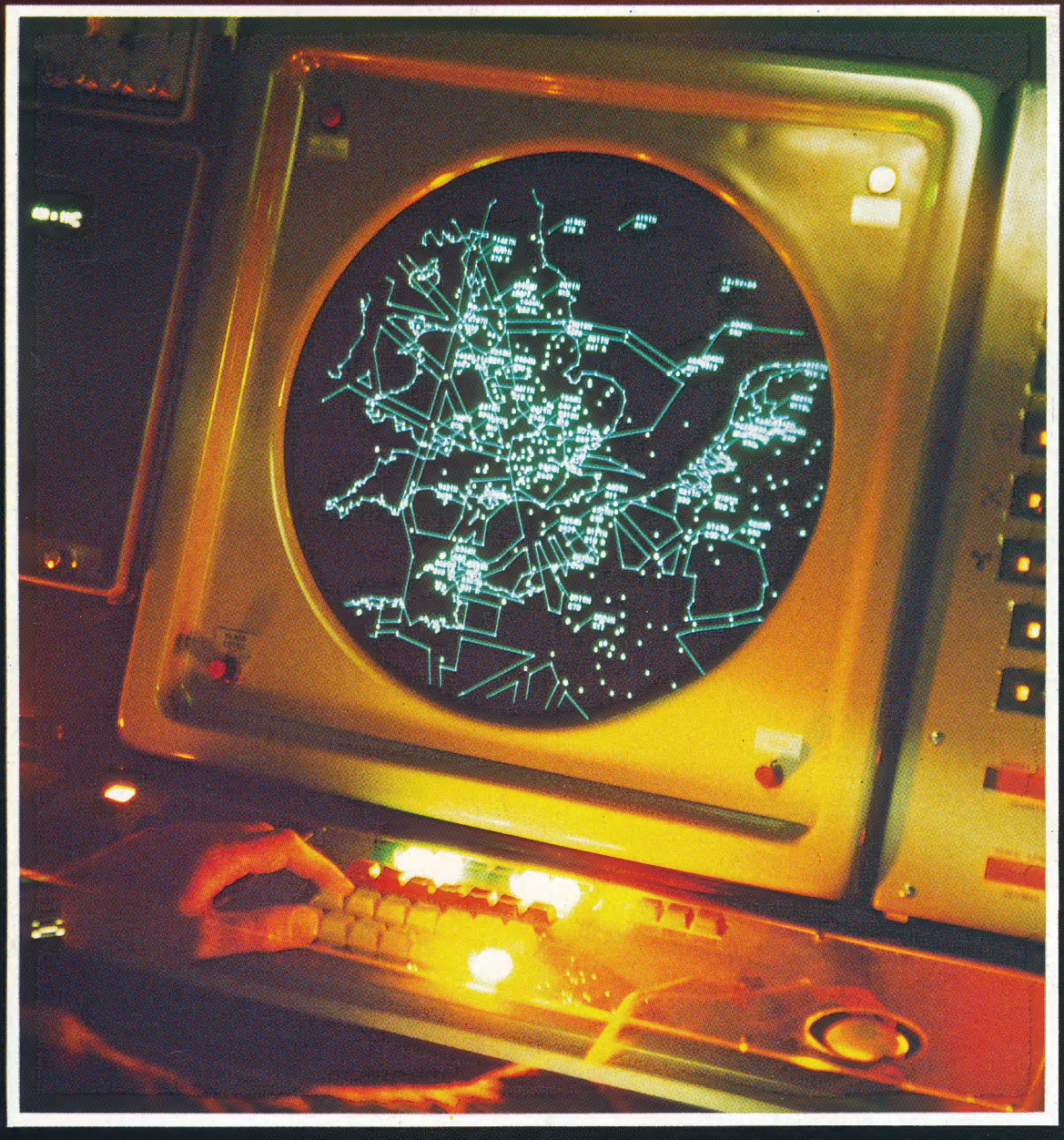

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20

DIGITAL ELECTRONICS

Analogue-to-digital conversion

ADCs

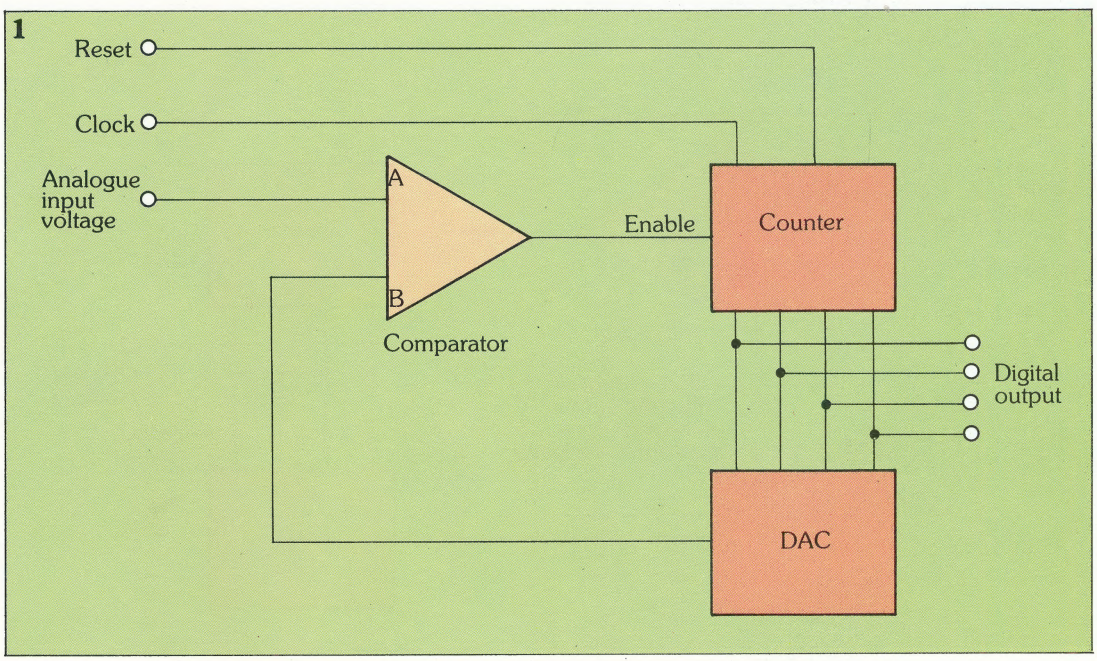
In *Digital Electronics 19* we saw how two basic digital-to-analogue converters can be made from a handful of resistors and a buffer amplifier. Digital codewords of any number of bits can be converted to a varying analogue signal using one of these two simple circuits.

Circuits used to perform the opposite function, i.e. analogue-to-digital conversion, are inherently more complex than DACs – often, in fact, DACs are used within ADCs – and for this reason we will not be concerned with actual circuit details, but instead will concentrate on overall principles, presented in block diagram form. You will be familiar with many of the circuit blocks as they have been discussed in previous chapters – new circuits will also be introduced. Although these new circuit blocks will be covered in detail in future *Solid State Electronics* chapters, their basic operation must be appreciated in order to understand ADC operation.

We will first take a simple example, introducing us to a new principle and thereby enabling the construction of improved but more complex examples.

Counter-type ADCs

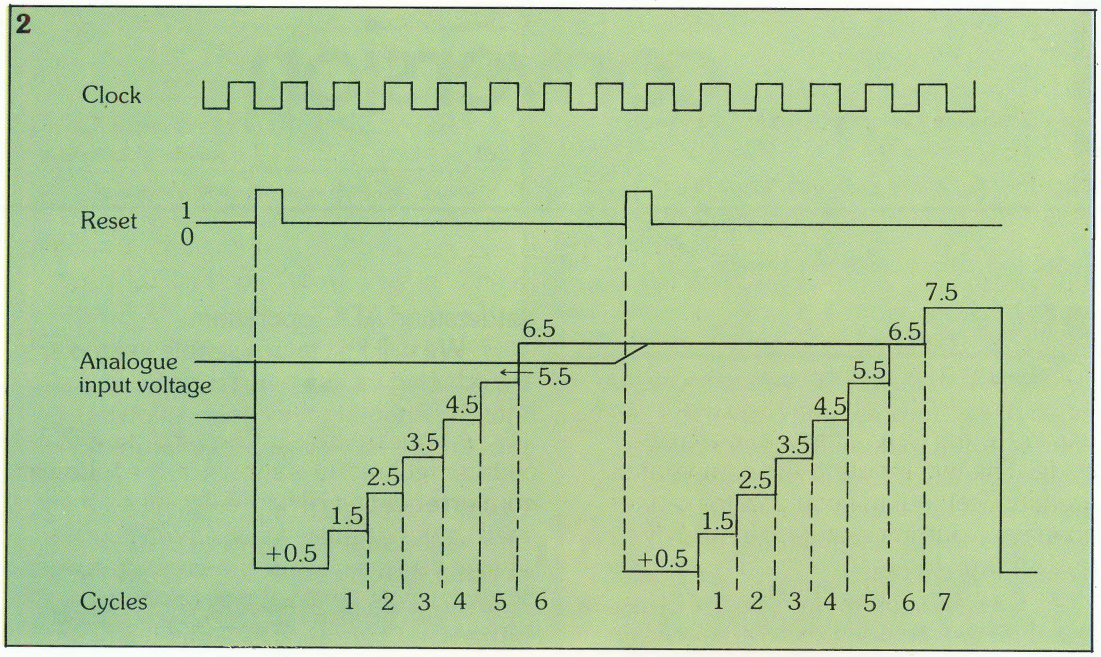
One of the simplest types of ADC, the **counter-ramp converter**, is shown in *figure 1*. Two of the blocks in the counter-ramp converter, the DAC and the counter, we have already met but the third, a **comparator**, is new to us.



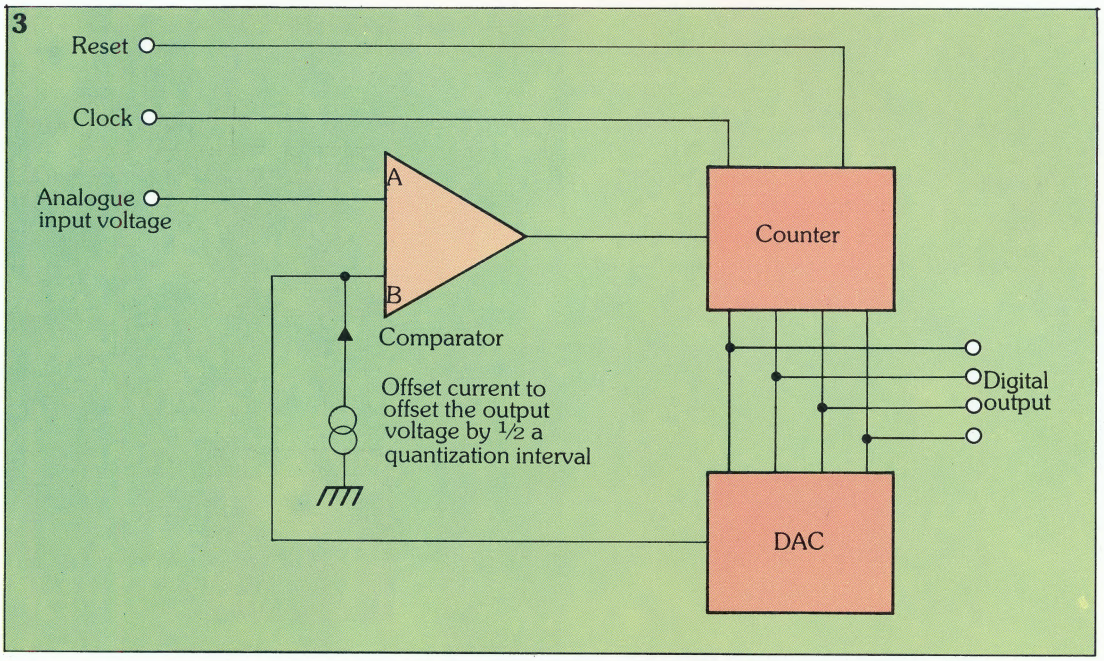
1. A counter-ramp converter comprising three circuit blocks: counter, DAC and comparator.

A comparator is a device with two inputs and one output which compares the voltages at each input to determine which is greater; the output of this converter is logic 1 if input A is larger than input B, and is logic 0, if input B is larger than input A.

We may understand circuit operation if we first assume that a reset signal is sent to the counter resetting it to zero. A constant DC voltage, which may be sup-



2. Timing diagram for the circuit in *figure 1*.



3. Reducing the quantization error of the circuit in *figure 1* by offsetting the output voltage.

plied by a sample-and-hold circuit, is then applied to input A of the comparator. As the counter output is zero, the DAC output voltage is 0 V, so the voltage at input A is greater than that at input B. The comparator output is therefore logic 1, enabling the counter, which begins to count the clock pulses.

As the counter increments at each clock pulse the digital output changes, and the DAC output voltage increases. For as long as this voltage is below the input voltage, the comparator output is 1 and the counter continues to increment. However, when the DAC output voltage increases to the point where it is higher than the input voltage, the comparator output becomes logic 0 which disables the counter. The digital output becomes fixed at a value corresponding to the analogue input voltage.

Figure 2 shows voltages at various points in the circuit in a timing diagram which illustrates clearly how the circuit functions over two analogue-to-digital conversions. The diagram also shows how

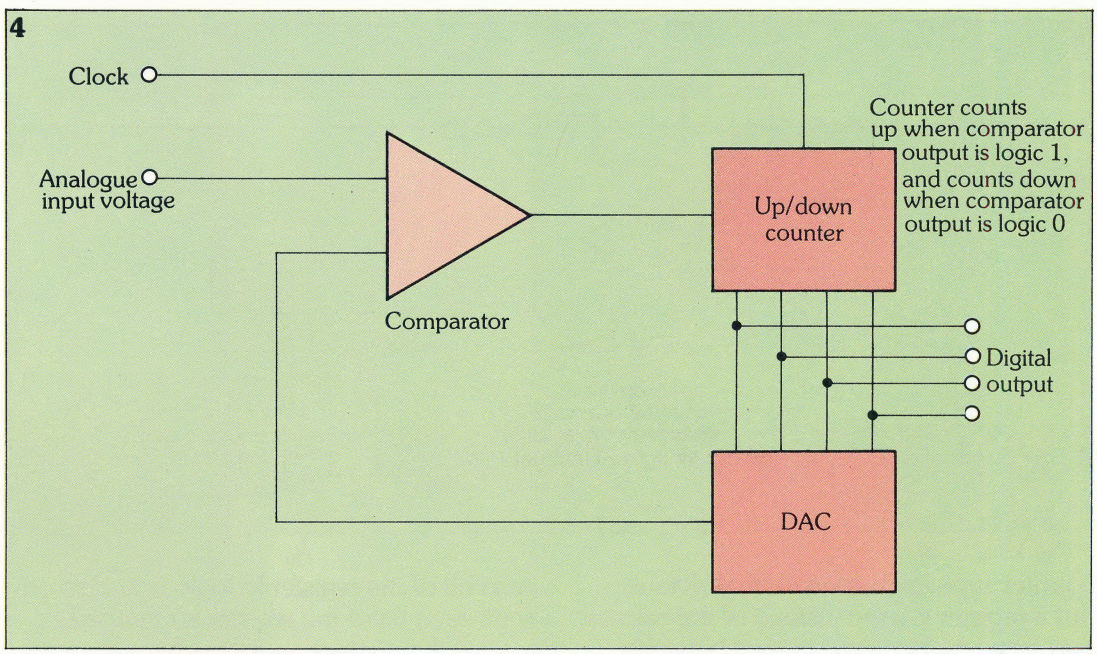
quantization errors occur in an ADC. In the case of the first conversion shown, the output voltages of the DAC at clock cycles 5 and 6 are equally spaced below and above the input voltage. When the final digital output is obtained, it is therefore at a quantization level of half a quantization interval above the corresponding analogue input voltage. The quantization error is thus half the quantization interval.

However, in the case of the second conversion, the analogue input voltage has increased slightly so that it corresponds *exactly* to the DAC output at the clock cycle. The two inputs to the comparator are identical, but the comparator cannot change its output state *until input B is greater than input A*, so the counter must increase through a further clock cycle until the DAC output is greater than the analogue input. The *maximum* quantization error which this circuit produces is therefore one whole quantization interval. This may be reduced, as shown in *figure 3*, by offsetting the output of the comparator by half the value of a quantization interval.

Offsetting was discussed in *Digital Electronics 19*: an offset current was provided at the input of a buffer amplifier causing a fixed offset voltage at the output. This may also be applied to a comparator. The offset principle, analogous to the rounding of a number up or down in arithmetic terms, is used in the majority of ADCs although it will not be included in any further circuits here.

Although the counter-ramp converter is very simple and has its advantages, it is slow in operation. The speed of operation is largely dependent on the speed of the counter and the DAC involved, but also on the number of cycles required until the DAC output voltage increases above the analogue input voltage. This means that the higher the analogue input voltage, the longer it takes to make a conversion.

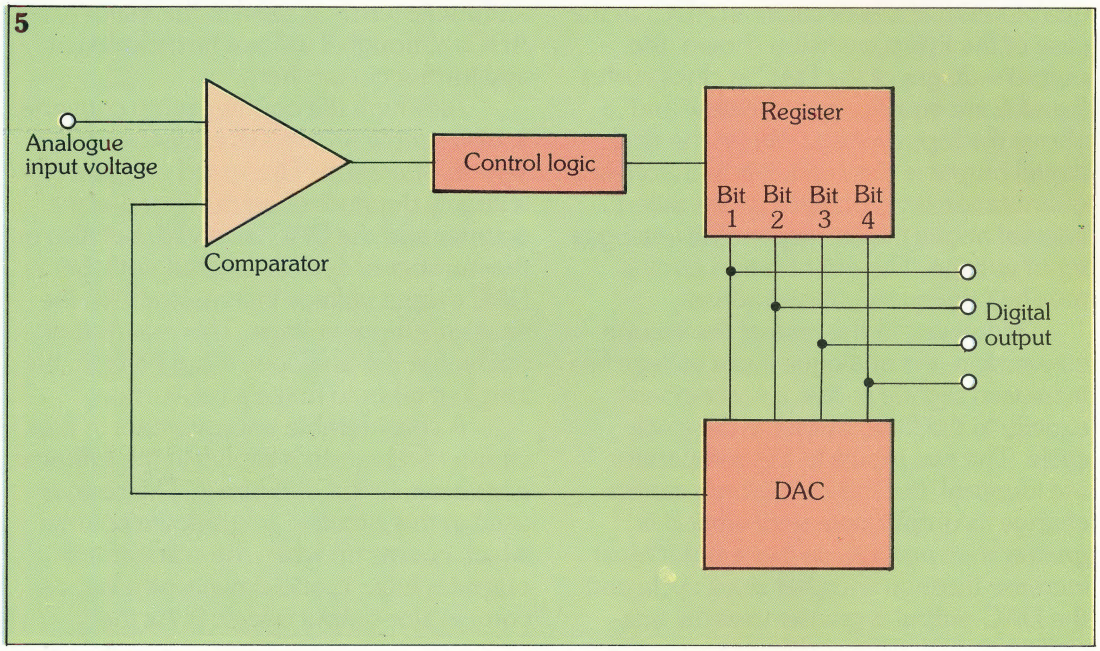
A considerable improvement in the counter technique is shown in the **follower converter** circuit of *figure 4*. The counter used in this circuit is an up/down counter which counts up when the comparator output is logic 1, and down when the comparator output is logic 0. As the analogue input voltage varies, the counter simply counts up or down from the previous count until the correct count is reached; a considerable improvement over the counter-ramp converter where the count starts from zero with every new applied analogue signal.



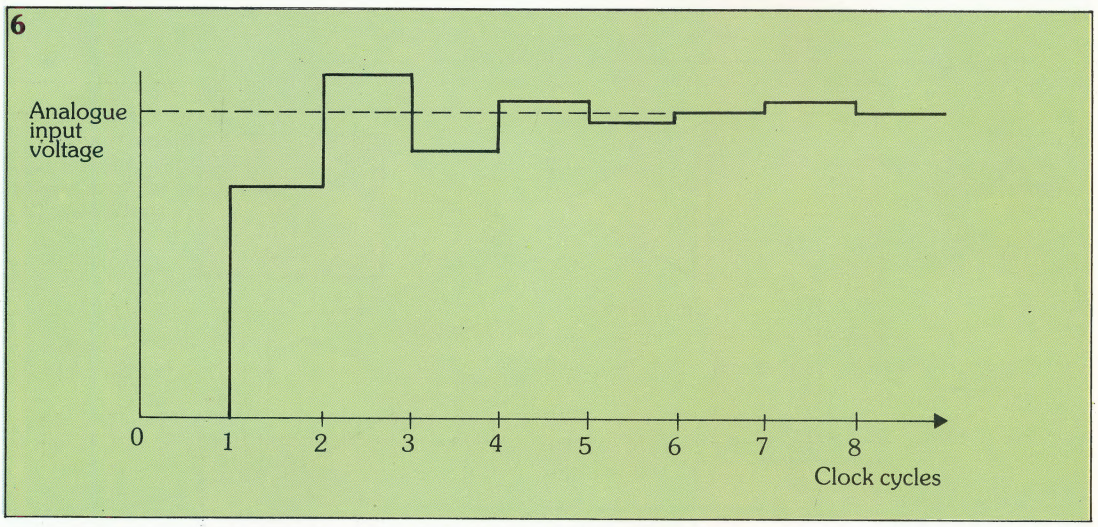
4. A following converter circuit which employs an up/down counter as the counter circuit block.

Successive approximation converter

One of the most popular types of ADC is the **successive approximation converter** an example of which is shown in *figure 5*. The circuit has a similar format to the



5. A successive approximation converter.



6. Timing diagram of a successive approximation conversion cycle of an 8-bit successive approximation ADC.

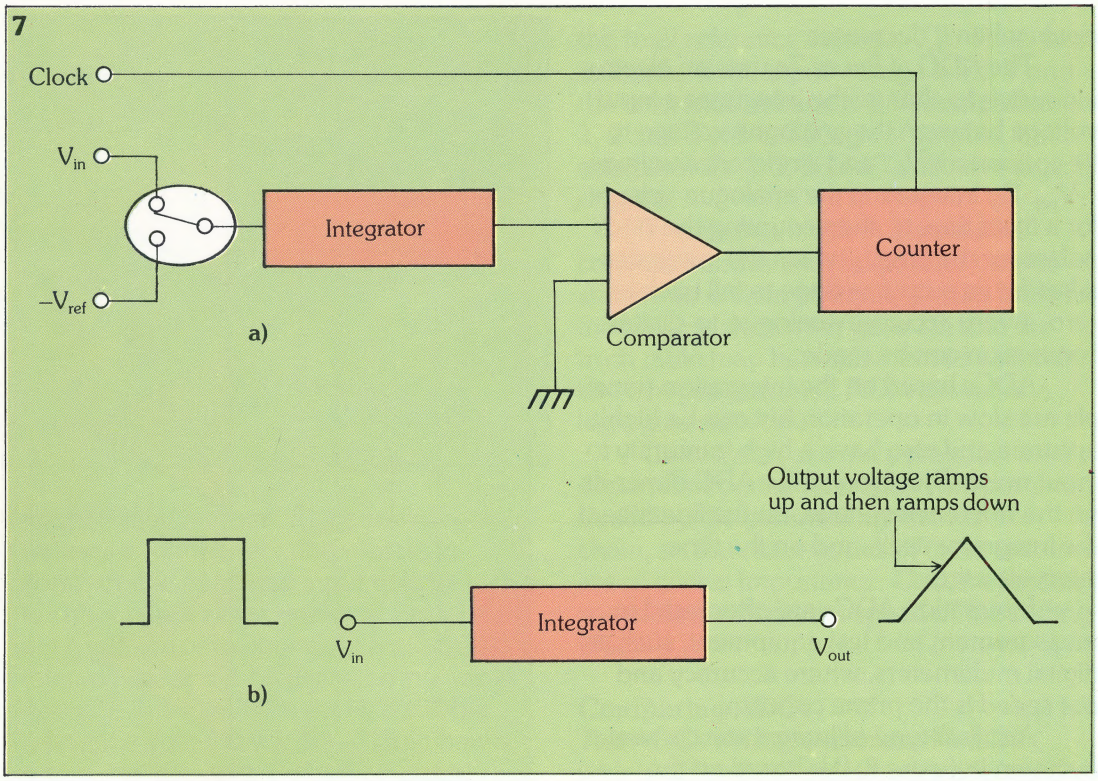
counter-type converters seen previously, but a register is used instead of the counter and an extra block is included between comparator and register which controls the outputs of the register.

Circuit operation is as follows. A reset signal initialises the circuit by setting all bits of the register to 0. The output of the DAC is thus 0 V and any applied analogue input signal causes the comparator output to be logic 1. The first clock pulse causes the control block to change the MSB of the register to 1, and so the DAC output increases. If the analogue input voltage is still higher than this, the output of the comparator remains at logic 1. At the next clock pulse, the control block changes the next bit of the register to logic 1, and so on until each bit of the register is changed.

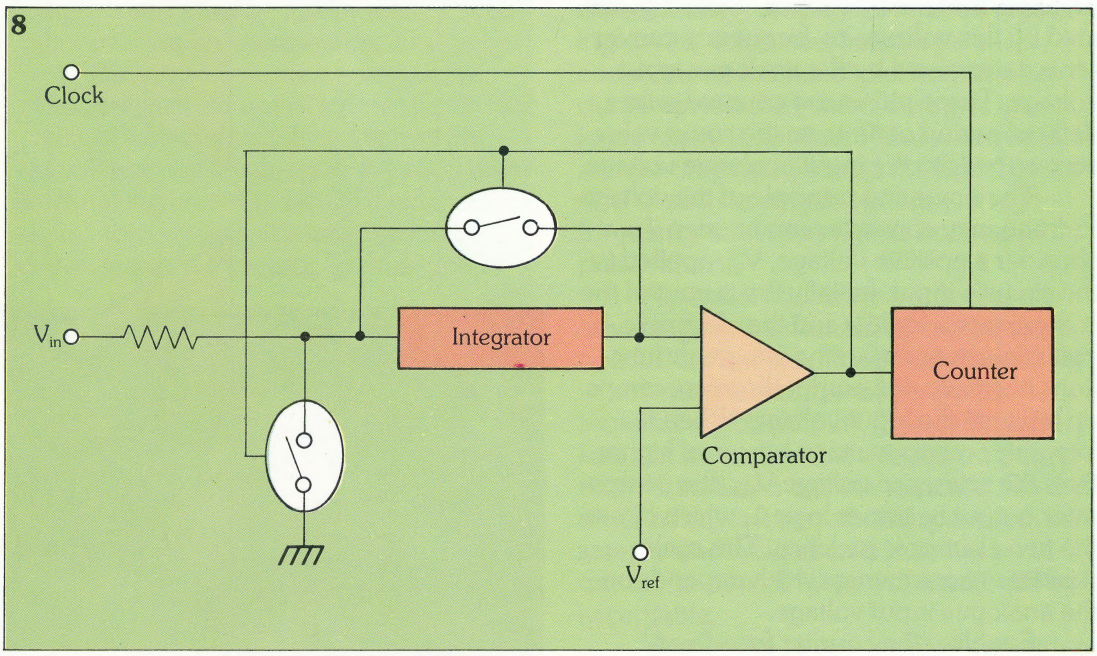
If the analogue input voltage after any of these **approximation** steps is lower than the DAC output voltage, the control block resets the last bit to 0 before changing the next bit to 1.

The total conversion time of a successive approximation converter is equal to N clock cycles, where N is the number of bits of the converter. This time is thus independent of the input voltages – unlike the conversion time of the counter-type ADCs.

Figure 6 shows a timing diagram of a successive approximation conversion cycle of an 8-bit successive approximation ADC.



7. (a) An ADC circuit utilising an integrator; **(b)** representation of input and output waves from an integrator.



8. A voltage-to-frequency converter.

Integration converters

Figure 7a shows the circuit of an ADC which uses an analogue circuit we have not yet studied – an **integrator**. The output voltage of an integrator varies not just as a function of the input, but also as a function of time. For example, if the input voltage of an integrator changes rapidly from 0 V to 5 V, it takes a time, t, for the output voltage to change from 0 V to 5 V. This can be seen in *figure 7b* where the input voltage is shown as a positive going pulse. Output of the integrator is a slowly changing voltage first increasing and then decreasing as the input changes. Voltages which increase and decrease like this are often termed **ramps**, and we may say that a voltage *ramps up* when it increases and *ramps*

down when it decreases.

The ADC of *figure 7a* uses an electronic switch to change the integrator's input voltage between the analogue voltage to be converted, V_{in}, and a reference voltage, $-V_{ref}$. By integrating the analogue voltage for a fixed time t_1, then counting the clock pulses for the time t_2 which the integrator takes for its output voltage to fall back to zero, a very accurate analogue-to-digital conversion can be made.

ADCs based on the integration principle are slow in operation but can be highly accurate and also have a high immunity to input noise. Precision of the ADC depends on the reference voltage, on the linearity of the integrator itself, and on the time intervals used.

Integration ADCs are often used in measurement and test equipment, such as digital multimeters, where accuracy and not speed is the prime concern.

Another type of integration converter is shown in *figure 8*. It is based on the principle that the frequency of pulse generated by this **voltage-to-frequency converter** is determined by the analogue input voltage. These pulses are counted over a defined period of time, so the count value corresponds to the input analogue voltage.

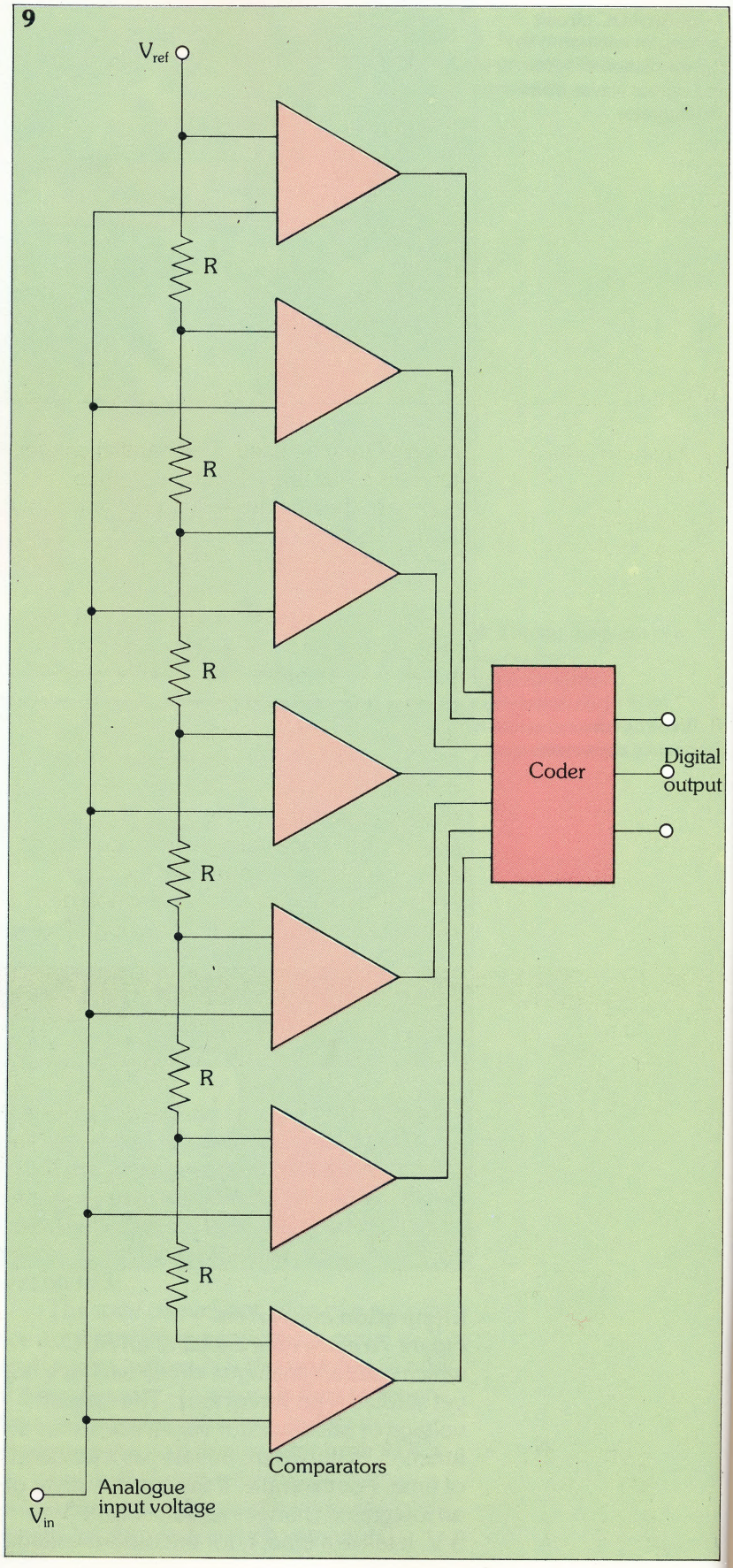
The operating principle of the voltage-to-frequency converter can be seen if we consider a positive voltage, V_{in}, applied to the circuit's input. Initially the output of the comparator is logic 0 and the electronic switches are open, so the integrator functions normally. It's output therefore ramps up towards the input voltage. When the integrator output voltage becomes higher than the reference voltage V_{ref}, the comparator output becomes logic 1, which closes the two electronic switches. This cycle repeats at a frequency which depends on the analogue input voltage.

Enabling the counter for a fixed period of time allows a count to be made of the number of cycles of the voltage-to-frequency converter. This count is therefore dependent on the analogue input voltage.

Parallel converter

Where high speed of operation is required a **parallel converter**, also known as a **flash converter**, such as the example in

9



10

Inputs from comparators							Digital output		
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

9. A parallel or flash converter.

10. Truth table for the coding block in a parallel converter.

figure 9 may be used. The parallel converter uses a number of comparators to compare the analogue input voltage with a number of reference voltages. Each reference voltage corresponds to a quantization interval, so for a 3-bit digital output (as in *figure 9*) there must be seven available reference voltages (i.e. 2^3-1) and hence seven comparators. For a 4-bit digital output there must be fifteen reference voltages and fifteen comparators, and so on.

The seven reference voltages are obtained with the use of a potential divider chain of resistors connected across the overall reference voltage. If the eight resistors making up the potential divider are equal, the voltages at each junction between resistors increases by an eighth of the total reference voltage, V_{ref}. Thus, for example, if the input voltage is 3.5 V and the reference voltage is 8 V, comparators 1, 2 and 3 will have logic 1 outputs, but comparators 4, 5, 6 and 7 will have logic 0 outputs.

The coding block in the parallel converter codes the comparator output states into a binary output. A truth table for the block is shown in *figure 10*, and the truth table may be implemented with the use of a programmed ROM device or a logic gate network.

Conversion accuracy is almost totally dependent on the reference voltages produced by the potential divider resistor chain, so the exact values of these resistors are of critical importance. Circuit operating speed depends on the speed of the coding block.

Below: process control in a rolling mill. Analogue signals from the various processes are converted to digital signals by ADCs.

The Research House/ASEA

Comparing ADCs

The ADCs we have discussed exhibit widely different characteristics and applications. Usually, they are compared regarding speed: the fastest being a parallel converter where the digital output is produced almost the instant the input analogue signal is applied. Parallel converters are the only type suitable for digital conversion of such analogue voltages as high frequency television signals and radar pulse returns.

A parallel converter's only real disadvantage is the number of comparators needed for low quantization errors (2^n-1): where n is the number of bits in the required digital output). These comparators can be costly where digital outputs of more than 4 or 5 bits are required. On the other hand, fast conversion speeds mean sample-and-hold circuits may not be required, so overall system cost may still be acceptable.

Successive approximation converters form the next fastest type of ADC. Their inherent simple construction and high resolution makes them an ideal choice in low-cost, medium-speed, medium-quality applications.

Counter converters, and in this group we shall include integrator converters, exhibit slow operating speeds. However, they can be extremely accurate and their simplicity is reflected in their low cost.

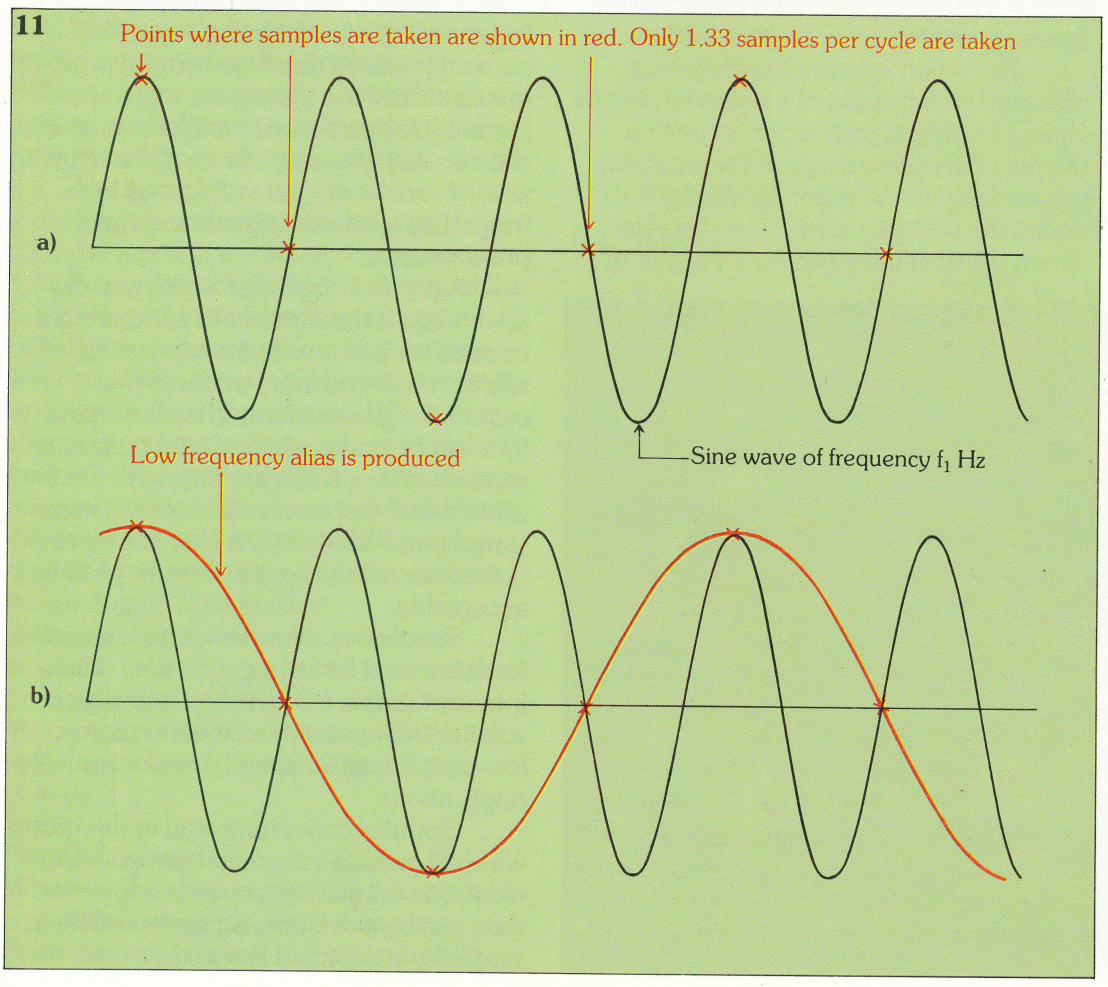
Aliasing

In the general discussion on sampling in *Digital Electronics 19* we saw that the sampling rule is used to define the rate at which the analogue input voltage of an ADC must be sampled before it may be converted to digital codewords. If, for example, an analogue signal consists of frequency components in the range from DC to f_{max} Hz, then it must be sampled at a rate of 2 f_{max} samples per second in order that it may be correctly recreated after processing.

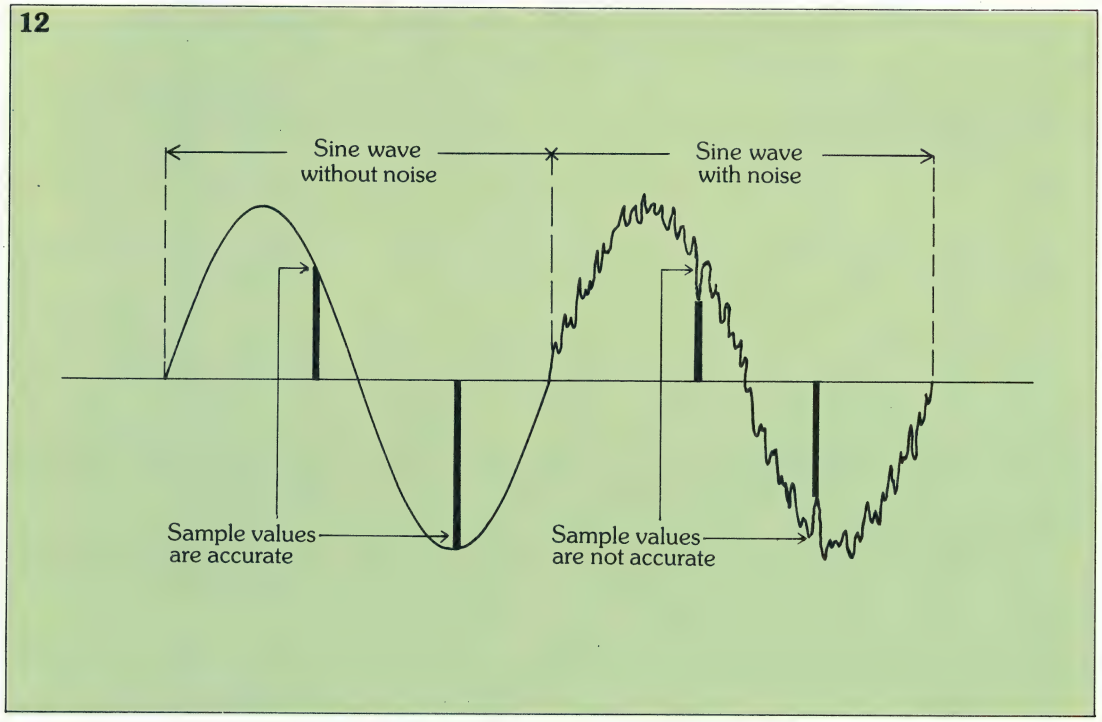
Figure 11a shows a sine wave of frequency f_1 Hz, which is sampled at a rate of only 1.33 samples per cycle. The problem with sampling at such a low rate is, as *figure 11b* shows, that *extra components are also produced* (and not that the original sine wave is not produced, as might have been expected). In this example, a second sine wave of frequency 0.33 f_1 Hz has been recreated along with the

The Research House/Philips

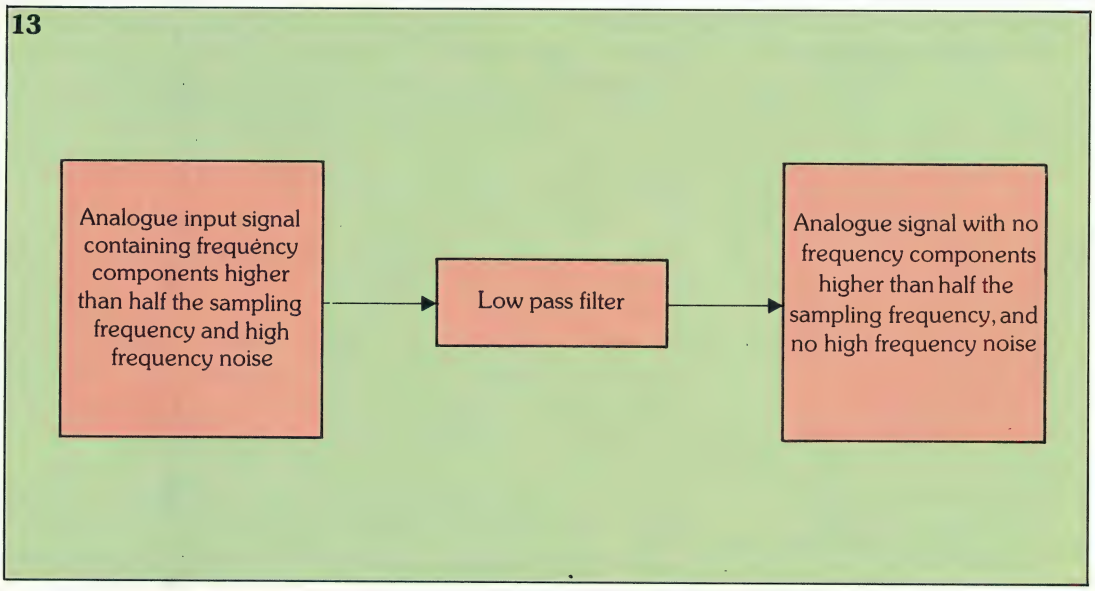
Above: a Philips laser disk. Analogue video signals are recorded onto the disk in video form using an ADC. The laser disk system then reconverts the digital signal into an analogue video signal.



11. (a) Sine wave sampled at a rate of 1.33 samples per cycle; **(b)** low frequency alias of the original wave produced by sampling at the low rate shown in (a).



12. The presence of noise affects the values of the samples taken, thereby introducing error.



13. Action of a low-pass filter.

original sine wave of frequency f_1 Hz. The second sine wave is known as a lower frequency **alias** of the original and is a form of error which must be prevented.

Another form of error occurs when high frequency noise is present. A possible example is shown in *figure 12* where an applied sine wave input is sampled four times. High frequency noise has been added to the second cycle of the sine wave and we can see that the presence of this noise affects the values of the samples taken.

The first of these types of error may be prevented and the second reduced by limiting the range of frequencies present in the signal which is to be sampled, so that no frequency components are sampled above half the sampling rate. A special type of analogue circuit known as a **low-pass filter** is used, as shown in *figure 13*, which filters out undesired higher frequency components, but allows low frequencies to pass through unhindered. A low-pass filter used in this way is often known as an **anti-aliasing filter**.

Glossary

alias	extra frequency components produced, for example, when an analogue signal is sampled at too low a rate. Aliasing is a form of error which analogue-to-digital and digital-to-analogue conversions may suffer from
anti-aliasing	a low-pass filter, introduced to an ADC system, which ensures that the analogue signal to be sampled has no frequency components above half the sampling frequency
approximation steps	steps taken by a successive approximation ADC in the digital estimation of the input analogue signal
comparator	analogue circuit which compares the voltages applied to each of its two inputs. The comparator output state depends on which of the two inputs is at a higher voltage
counter-ramp converter	an ADC circuit in which a comparator output enables or disables a counter, depending on whether the analogue input is greater than the digital-to-analogue converted count or not
follower converter	type of counter ADC in which the counter is of the up/down variety. This eliminates the requirement of resetting the counter to zero before commencing an analogue-to-digital conversion
integrator	analogue circuit whose output varies as a function of the input *and* as a function of time
low-pass filter	analogue circuit which passes low frequency components but removes high frequency components
parallel converter, flash converter	an ADC in which the input analogue signal is simultaneously compared with a number of reference voltages corresponding to quantization intervals. Uses $2^n - 1$ analogue comparators where n is the number of required bits in the digital output
successive approximation converter	an ADC in which the digital output is estimated N number of times, where N is the number of required bits in the digital output. By comparing a digital-to-analogue converted signal of each approximation with the input analogue signal, before proceeding with the next approximation, an accurate analogue-to-digital conversion may be made

ELECTRICAL TECHNOLOGY

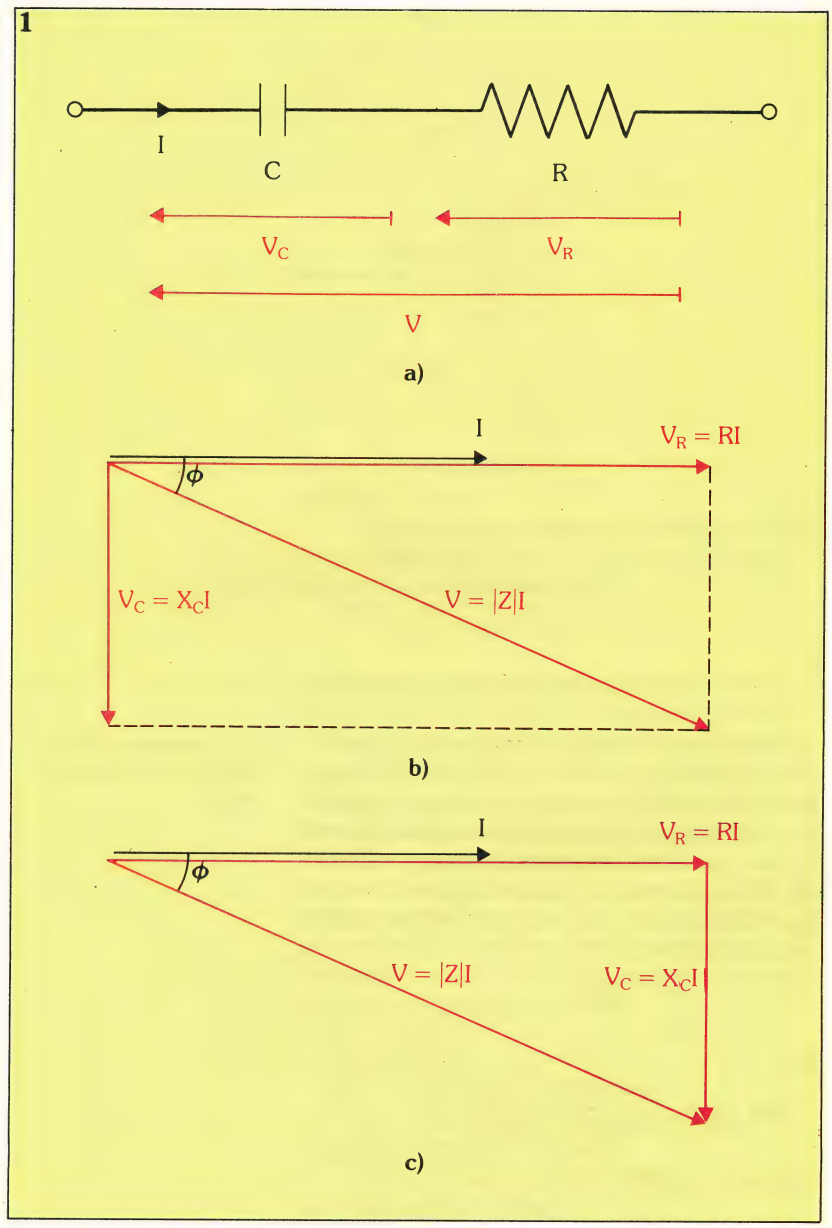
AC in series circuits

We have looked at the relationship between current and voltage in simple circuits, and at the way in which real circuits can be modelled. We will now consider circuits in which two or more elements are connected in series.

Capacitor and resistor in series

Looking at *figure 1*, we can see that the alternating sinusoidal current flowing through the resistor, is the same as that through the capacitor. Also, the total voltage across the circuit is the sum of the voltages across the resistor and the capacitor separately.

1. A capacitor and a resistor in series.



However, we must remember that we can either add the two voltages at every instant in time, or we can represent these alternating sinusoidal voltages by phasors of their rms values, and use the rules for the addition of phasors to obtain the rms value of the total voltage. This has been done in *figure 1b*, where the rms value of the current, I, is our reference phasor. V_R, the voltage across the resistor, is then constructed in phase with I, where:

$$V_R = RI$$

Similarly, V_C, the voltage across the capacitor, lags the current by 90°, where:

$$V_C = X_C I$$

X_C is the reactance of the capacitor, and this is given by:

$$X_C = \frac{1}{2\pi fC}$$

where f is the frequency of the supply current or voltage.

The parallelogram can then be completed and the resultant, V, can be drawn: this is the voltage across the complete circuit. If we let Z represent the total impedance of the circuit, then:

$$V = ZI$$

We have, so far, added our phasors using the parallelogram rule, but looking at *figure 1c*, we see that the same result is obtained by drawing the two phasors V_C and V_R in the form of a triangle – with the tail of one phasor joined to the head of the previous phasor. The total voltage is now found by joining the starting end of this string of phasors to the end point, as shown.

We can, in fact, continue this with any number of phasors which we may wish to add together – simply by drawing them head to tail and then joining the starting point to the end point to give the total phasor.

Looking at the triangle of *figure 1c* we see that using Pythagoras' theorem:

$$V^2 = V_R^2 + V_C^2$$

Substituting with the expressions above we obtain:

$$Z^2 I^2 = R^2 I^2 + X_C^2 I^2$$

and dividing by I^2 gives us:

$$Z^2 = R^2 + X_C^2$$

$$Z = \sqrt{R^2 + X_C^2}$$

If we were to draw a diagram, similar to the voltage phasor diagram, for this expression, connecting impedance with resistance and reactance, we would see that the phase angle between voltage and current in this circuit is given by the expression:

$$\tan \phi = \frac{X_C}{R} = \frac{V_C}{V_R}$$

which shows us that the current is leading the supply voltage.

Inductor and resistor in series

Figure 2a illustrates a slightly more complex circuit with a resistor and inductor connected in series. We have seen that a real inductor can be modelled by an ideal inductor in series with an ideal resistor, and this is shown in *figure 2b* inside the red box.

Let's take a numerical example to see how this works. The inductor may be modelled by an inductance, L, of 79.6 mH connected in series with a resistor, R_L, of 10 Ω, which, in turn, is connected in series with a separate resistor, R, of 20 Ω. A current of 2 A flows through the circuit at a frequency of 50 Hz.

The phasor diagram shown in *figure 2c* can now be drawn, starting with the current as the reference phasor of length 2 units. The reactance of the ideal inductance is given by:

$$X_L = 2\pi fL = 2 \times \pi \times 50 \times 79.6 \times 10^{-3} = 25\ \Omega$$

We can draw a phasor, V_L, leading the current by 90° and of rms value:

$$V_L = X_L I = 25 \times 2 = 50\ V$$

The phasor, V_{RL}, can be drawn in phase with the current (parallel to the current) in the same way. This is given by:

$$V_{RL} = R_L I = 10 \times 2 = 20\ A$$

The voltage across the inductor can then be found by:

$$V_{IND} = \sqrt{V_L^2 + V_{RL}^2} = \sqrt{50^2 + 20^2} = 53.9\ V$$

at a phase angle ϕ, given by:

$$\tan \phi = \frac{50}{20} = 2.5$$

and so the phase angle $\phi = 68°$.

The voltage across the resistor in phase with the current can now be drawn to join the end of V_{IND}, and this is given by:

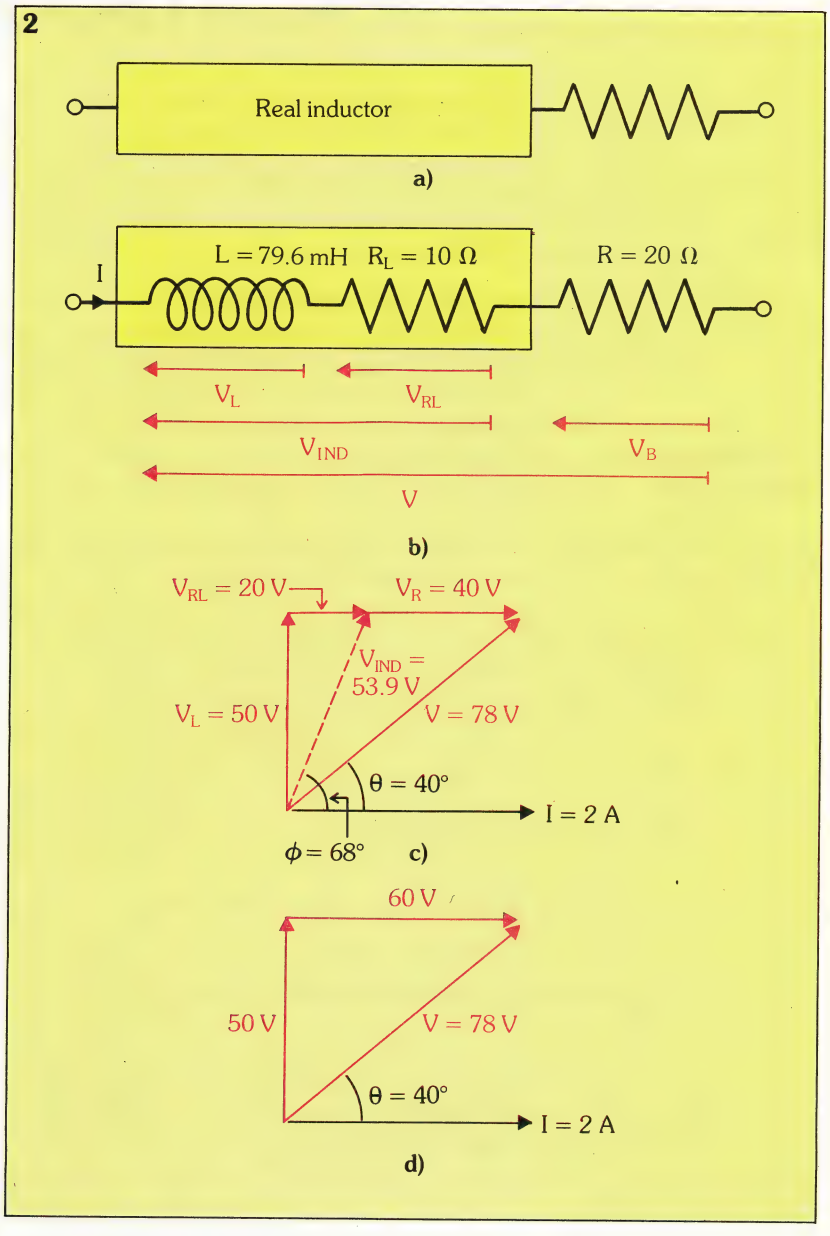
$$V_R = RI = 20 \times 2 = 40\ V$$

Adding V_{IND} and V_R gives the total voltage where its magnitude, V, and phase angle, θ, are found (by measurement from the phasor diagram) to be: V = 78 V and $\theta = 40°$. From this, we can add together the in phase voltages V_{RL} and V_R giving a total in phase voltage of 60 V. Along with the one reactive voltage of 50 V, we can then draw the phasor diagram shown in *figure 2d*. V and θ can now be mathematically calculated from:

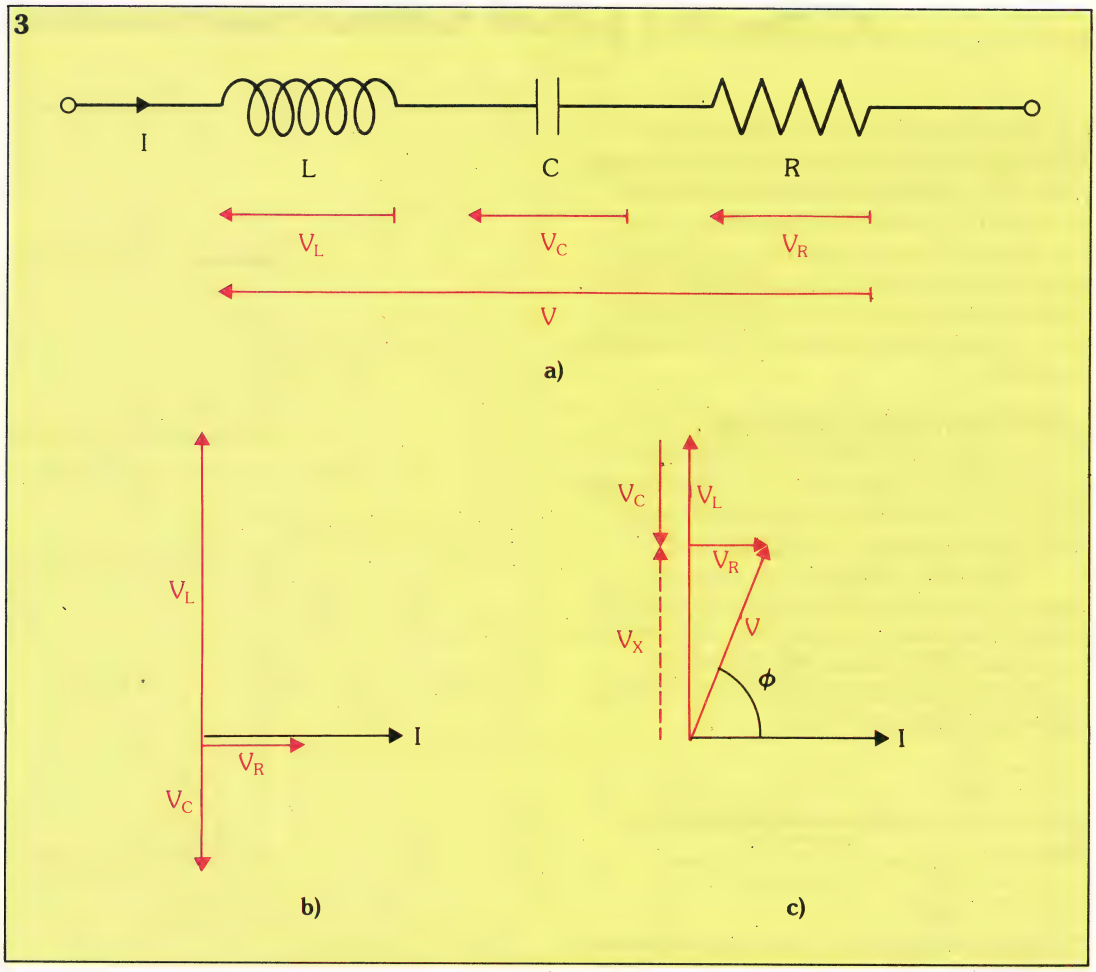
$$V = \sqrt{50^2 + 60^2} = 78\ V$$

and:

$$\tan \theta = \frac{\text{quadrature voltage}}{\text{in phase voltage}} = \frac{50}{60}$$



2. A resistor and an inductor connected in series.



3. A resistor, capacitor and inductor in series.

$$= 0.8333$$

giving: $\theta = 40°$.

Quadrature voltage is a voltage at 90° to the current. Note than tan θ is also given by:

$$\tan\theta = \frac{\text{total reactance}}{\text{total resistance}}$$

Inductor, capacitor and resistor in series

Figure 3a shows a circuit comprising an ideal inductor, capacitor and resistor connected in series. We start with the current, I, that is flowing through the circuit as the same amount flows through each element. We may now draw the phasor diagram for the voltage across the inductor, V_L, leading the current by 90°; the voltage across the capacitor, V_C, lagging the current by 90°; and the voltage across the resistor, V_R, which is in phase with the current, as shown in *figure 3b*, where:

$V_L = X_L I$
$V_C = X_C I$
$V_R = RI$

The total voltage is found by adding these together as shown in *figure 3c*.

Adding the quadrature voltages gives us the total reactive voltage, V_X:

$$V_X = V_L - V_C$$

Adding this value to the in phase voltage, V_R, gives the total voltage, V, where:

$$V = \sqrt{V_X^2 + V_R^2}$$

at a phase angle ϕ, where:

$$\tan\phi = \frac{V_X}{V_R}$$

The phase angle is such that the voltage leads the current if the reactance of the inductor is greater than that of the capacitor. On the other hand, if the reactance of the capacitor is greater, the voltage lags the current.

Summary

We can generalise what we have just done for a circuit containing many components. Starting with the current, we draw phasors to represent the voltage across each element of the circuit at the appropriate phase angle; these are then all added together to give the total voltage across the circuit. The simplest way of doing this is to add all the in phase voltages and the quadrature voltages separately, and then to combine these using the phasor triangle. □

BASIC THEORY REFRESHER

ELECTRICAL TECHNOLOGY

AC in parallel circuits

We will now turn our attention to the relationship between current and voltage in circuits comprising a number of elements connected in parallel to a sinusoidal voltage. The approach is very similar to that used in series circuits, except that we shall start with the voltage as our reference phasor because the same voltage exists across each of the parallel elements.

Resistor and capacitor in parallel

As an example, consider the circuit shown in *figure 1a* where a capacitor, C, in parallel with a resistor, R, is connected across a sinusoidal voltage of rms value, V, at a frequency, f.

Taking the voltage as our reference phasor in *figure 1b*, we first derive the current through the resistor, I_R, and draw a phasor of magnitude V/R in phase with the voltage. Second, the current through the capacitor, I_C, can be calculated as follows:

$$I_C = \frac{V}{X_C}$$

where X_C is the reactance of the capacitor, given by:

$$X_C = \frac{1}{2\pi fC}$$

The phasor representing this is drawn so that it leads the voltage by 90°.

Finally, we use the rule for summation of phasors to give the total current, I. As with the series circuits previously looked at, these may be drawn end to end giving the total current as in *figure 1c*. From this we can see that the total current is of magnitude:

$$I = \sqrt{I_R^2 + I_C^2}$$

and the phase angle, ϕ, is given by:

$$\tan\phi = \frac{I_C}{I_R} = \frac{\frac{V}{X_C}}{\frac{V}{R}} = \frac{R}{X_C} = 2\pi fCR$$

Impedance of a parallel circuit

We have previously defined the magnitude of the impedance, |Z|, of a circuit as:

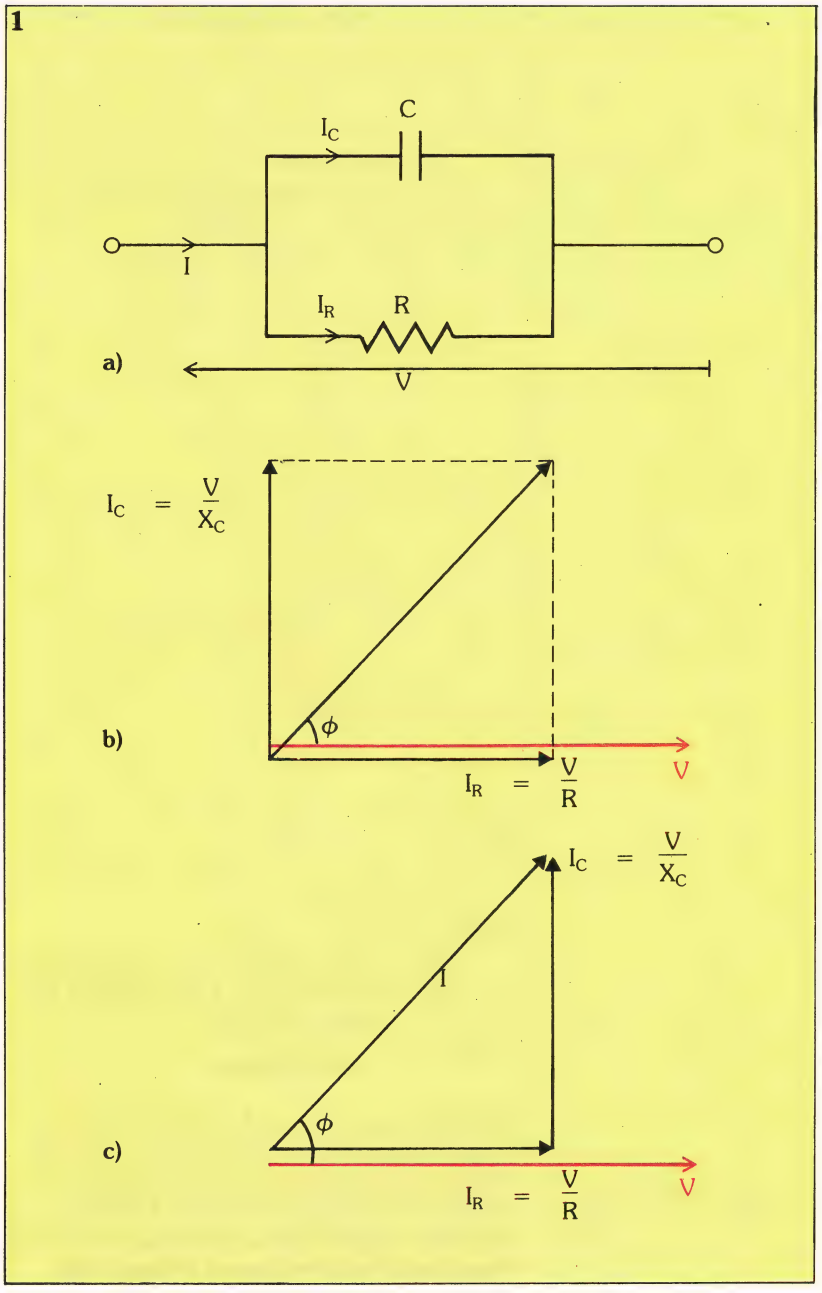
$$|Z| = \frac{V}{I}$$

and since:

$$I = \sqrt{I_R^2 + I_C^2}$$

we can write:

1



$$\frac{V}{|Z|} = \sqrt{\left(\frac{V}{R}\right)^2 + \left(\frac{V}{X_C}\right)^2}$$

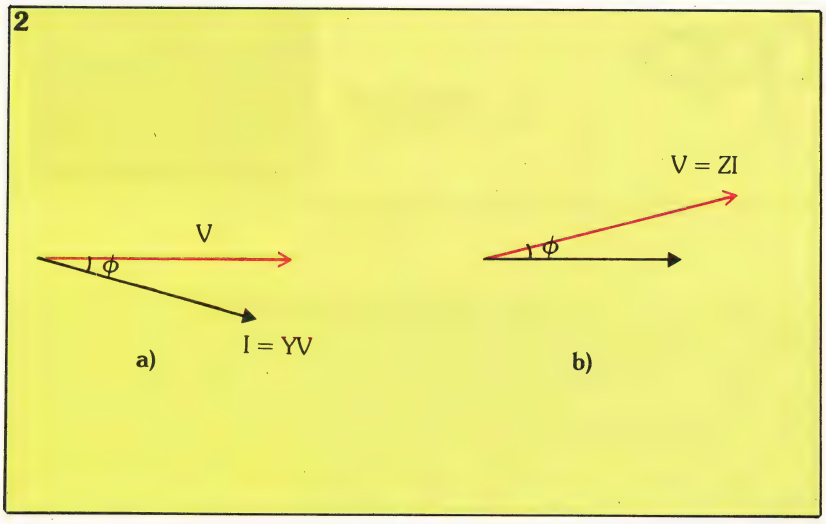
leading to:

$$\frac{1}{|Z|} = \sqrt{\frac{1}{R^2} + \frac{1}{X_C^2}}$$

The phase angle, ϕ, is obtained in the same way as above.

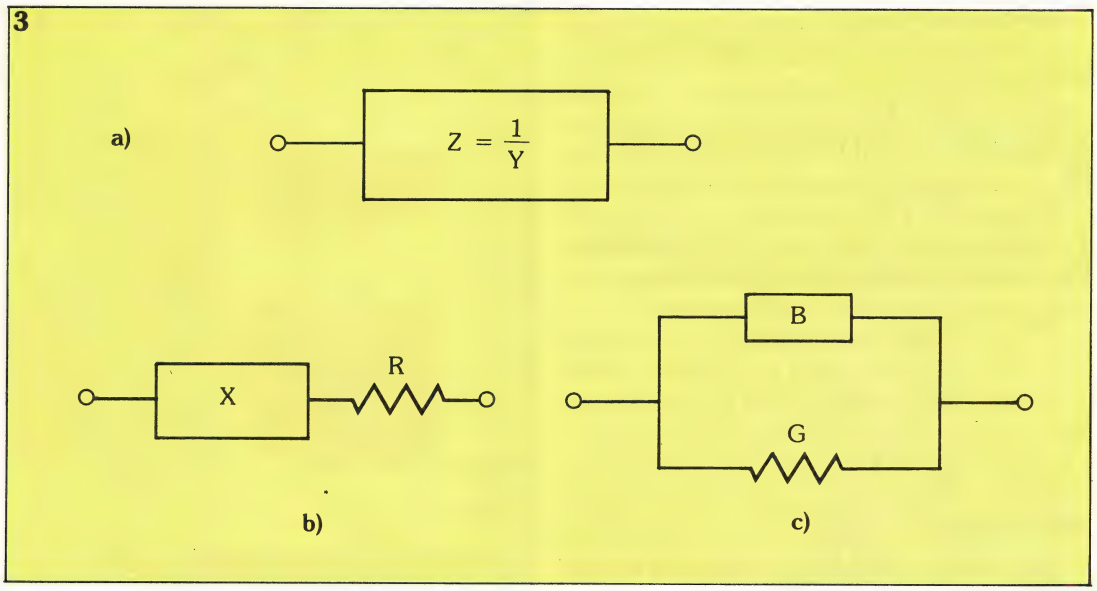
Admittance

Sometimes it is convenient to rewrite the equation for the generalised form of Ohm's law



1. A resistor and a capacitor in parallel.

2. Phasor diagram solution for a general circuit showing the: **(a)** resulting current; and **(b)** applied voltages.



3. Modelling the black-box circuit in **(a)** by either the series circuit in **(b)** or the parallel circuit in **(c)**.

in circuits using AC. So far, this has been written as:

$$V = |Z|\,I$$

where $|Z|$ is the magnitude of the impedance. We can write this alternatively as:

$$I = |Y|\,V$$

Here, $|Y|$ is termed the **admittance** of the circuit and is measured in Siemens. We can therefore see that:

$$|Y| = \frac{1}{|Z|}$$

So, the admittance of a circuit is the reciprocal of its impedance.

Conductance and susceptance

In the example looked at earlier, we saw that the current, I, was made up of two parts: I_R, in phase with the voltage, and I_C in quadrature with the voltage.

The ratio of the in phase current to the voltage is known as the **conductance**, G, which is also measured in Siemens. This means that:

$$I_R = GV$$

Similarly, the ratio of the quadrature current to the applied voltage is termed the **susceptance**, B. This is also measured in Siemens. Here, we have:

$$I_C = BV$$

From the fact that:

$$I = \sqrt{I_R^2 + I_C^2}$$

we see that:

$$|Y| = \sqrt{G^2 + B^2}$$

We may also see that in the circuit considered, the conductance of the resistor is:

$$G = \frac{1}{R}$$

and the susceptance of the capacitor is:

$$B_C = 2\pi fC$$

We may also show that the susceptance of an inductor is:

$$B_L = \frac{1}{2\pi fL}$$

Relationship between admittance and impedance

We may now compare a circuit described by admittance, conductance and susceptance, with one described by impedance, resistance and reactance. If we look at some general circuit, we can use either form of representation: if the circuit has a number of elements connected in *series*, it is more convenient to describe it by an impedance, since we add voltages together; if the circuit, on the other hand, consists of a number of elements connected in *parallel*, we may find that admittance is preferable.

However, at the end of any solution we end up with a phasor diagram as in *figure 2*. Here, only the applied voltages and the resulting currents are shown, as the parts of the diagram used for construction have been eliminated.

In many situations we may not be able to determine how a circuit is constructed as it may be sealed in a 'black-box', with only its terminals available. In this case, we can model the circuit in any way we choose, either as a series or a parallel circuit, depending on which phasor is chosen as the reference.

Figure 3a shows a black-box that has an impedance, Z, or an admittance Y. We can model this by the series connection of a resistance R and a reactance X, or, alternatively, by the parallel connection of a conductance G and a susceptance B.

Now, we know that the magnitude of the impedance is given by:

$$|Z| = \sqrt{R^2 + X^2}$$

and the magnitude of the admittance is given by:

$$|Y| = \sqrt{G^2 + B^2}$$

The phase angle of these two circuit models is the same (as shown in *figure 2*) and so:

$$\tan \phi = \frac{X}{R} = \frac{Y}{G}$$

As:

$$|Z| = \frac{1}{|Y|}$$

we also have:

$$R^2 + X^2 = \frac{1}{G^2 + B^2}$$

These equations enable us to find G and B from R and X, by:

$$G = \frac{R}{R^2 + X^2} \; ; \; B = \frac{X}{R^2 + X^2}$$

or, if we want R and X in terms of B and G, we have:

$$R = \frac{G}{G^2 + B^2} \; ; \; X = \frac{B}{G^2 + B^2}$$

This shows that we can represent quite a complicated circuit in the form of a model which may be either a simple series or parallel circuit.

Inductor, capacitor and resistor in parallel

As a final example of a parallel circuit we'll consider the connection of an ideal inductor, capacitor and resistor – as shown in *figure 4a*.

Taking the reference phasor to be the applied voltage, V, we can draw the current through the inductor, $I_L = B_L V$, lagging the voltage by 90°, where:

$$B_L = \frac{1}{2\pi f L}$$

In the same way, we can draw $I_C = B_C V$, leading the voltage by 90°, where:

$$B_C = 2\pi f C$$

Adding these two phasors head to tail we obtain the total quadrature current I_B. Now, inserting the current through the resistor as:

$$I_R = GV = \frac{V}{R}$$

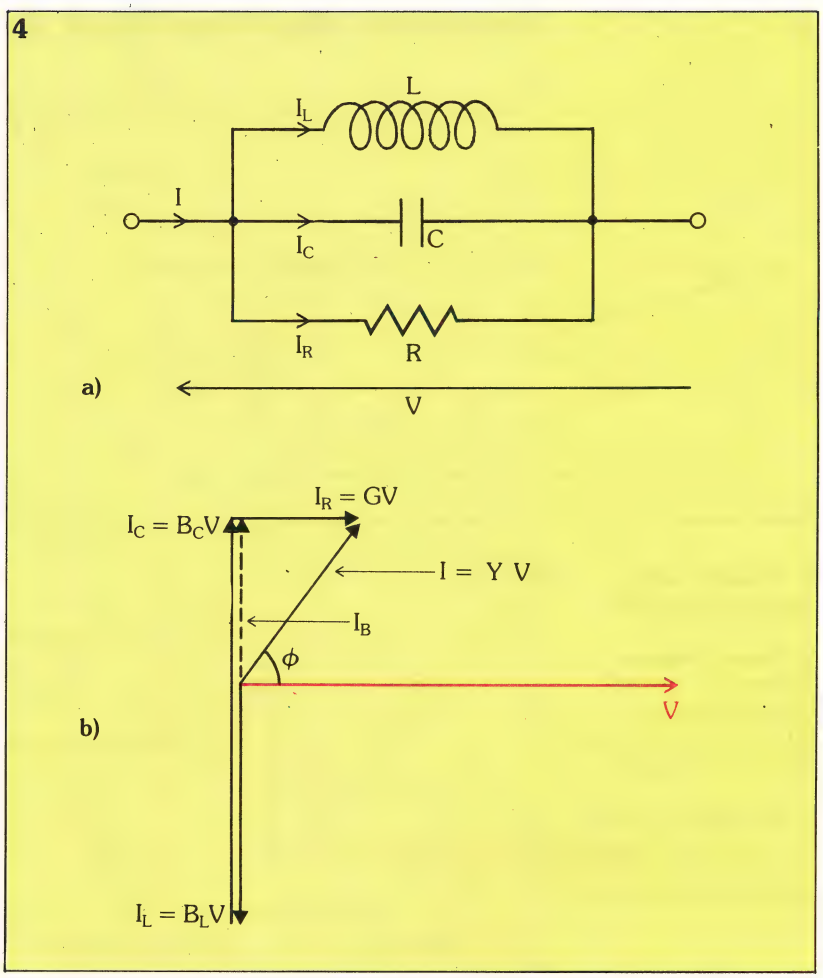
in phase with the voltage, enables the addition of these to give the total current, I, where:

$$I = \sqrt{I_R^2 + I_B^2}$$

This has a phase angle ϕ, given by:

$$\tan \phi = \frac{I_B}{I_R}$$

The current lags the voltage if I_L is greater than I_C, and vice-versa. □

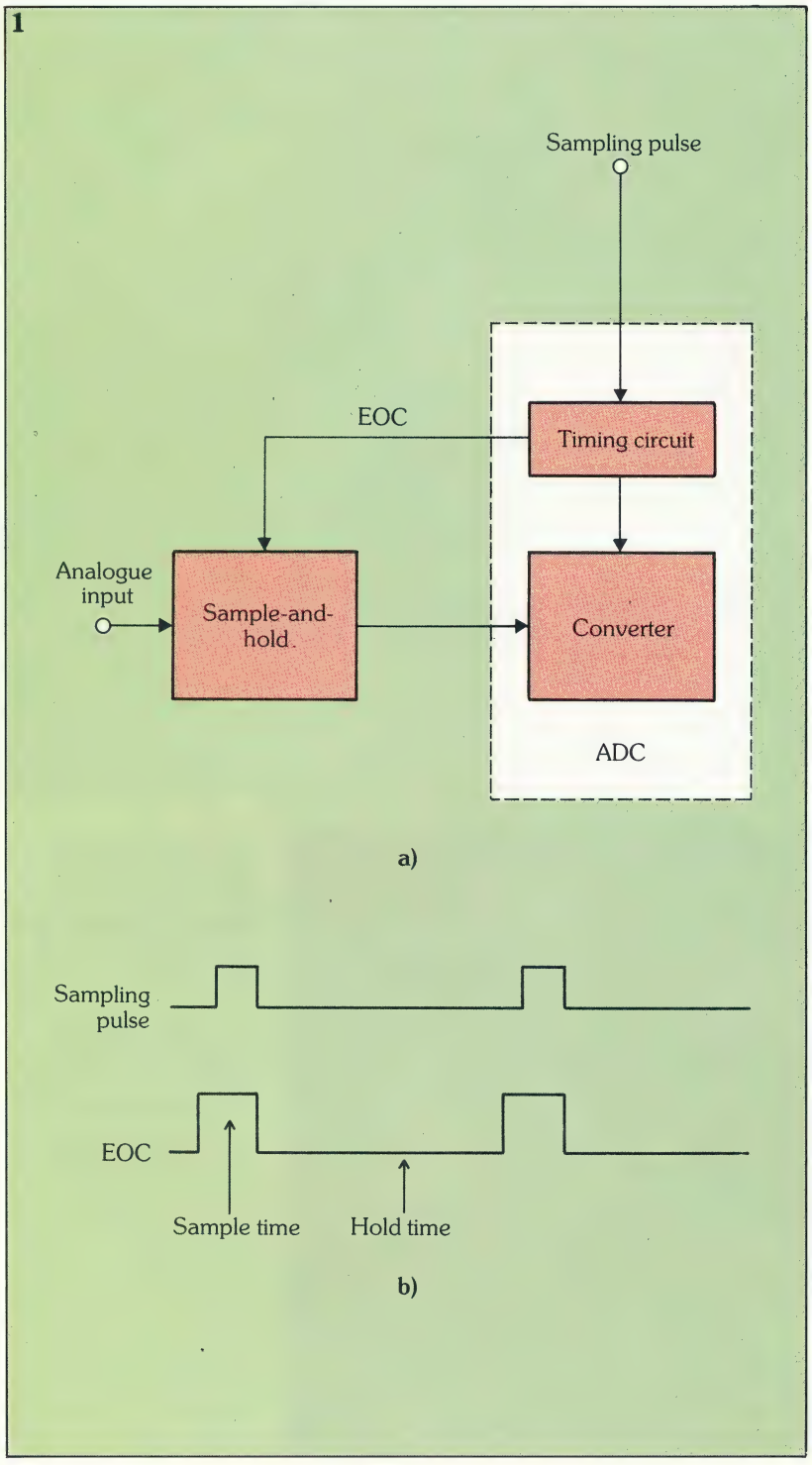


4. An inductor, capacitor and resistor in parallel.

21

DIGITAL ELECTRONICS

ADC and DAC applications



Interconnections between ADCs and sample-and-hold circuits

We saw in *Digital Electronics 20* that an analogue-to-digital conversion system does not consist only of an ADC. The two peripheral circuits we looked at were the sample-and-hold circuit and the anti-aliasing filter. An anti-aliasing filter is a simple analogue circuit which filters out unwanted frequency components from the analogue input signal before sampling takes place. It can thus be considered as a completely separate circuit block from the rest of the analogue-to-digital conversion system.

A sample-and-hold circuit, on the other hand, is a more complex circuit which, although it is also an analogue circuit, cannot be considered divorced from the conversion system. Its correct operation relies on a synchronised control signal which in many systems is generated by the ADC itself. In effect, the ADC must *tell* the sample-and-hold circuit when to take a new sample of the input signal, so that the required analogue-to-digital conversion may be accurately made. *Figure 1a* shows the interconnections between a sample-and-hold circuit and an ADC.

Note that the ADC is represented by two blocks: the first of which is the actual converter circuit and the second is a timing circuit. Depending on whether a counter-type, successive aproximation, or parallel converter is used, the timing circuit generates the necessary control signals, such as reset, bit setting, clock etc.

Input to the timing circuit is a single pulse, instructing it to sample, hold and convert an analogue input signal, thereby providing the digital output required. The timing circuit, apart from supplying all the necessary control signals to the converter, therefore also generates a control signal to

the sample-and-hold circuit – the **end of conversion signal** (EOC) – which operates the sampling switch. *Figure 1b* shows a timing diagram of the sampling pulse and the EOC signal.

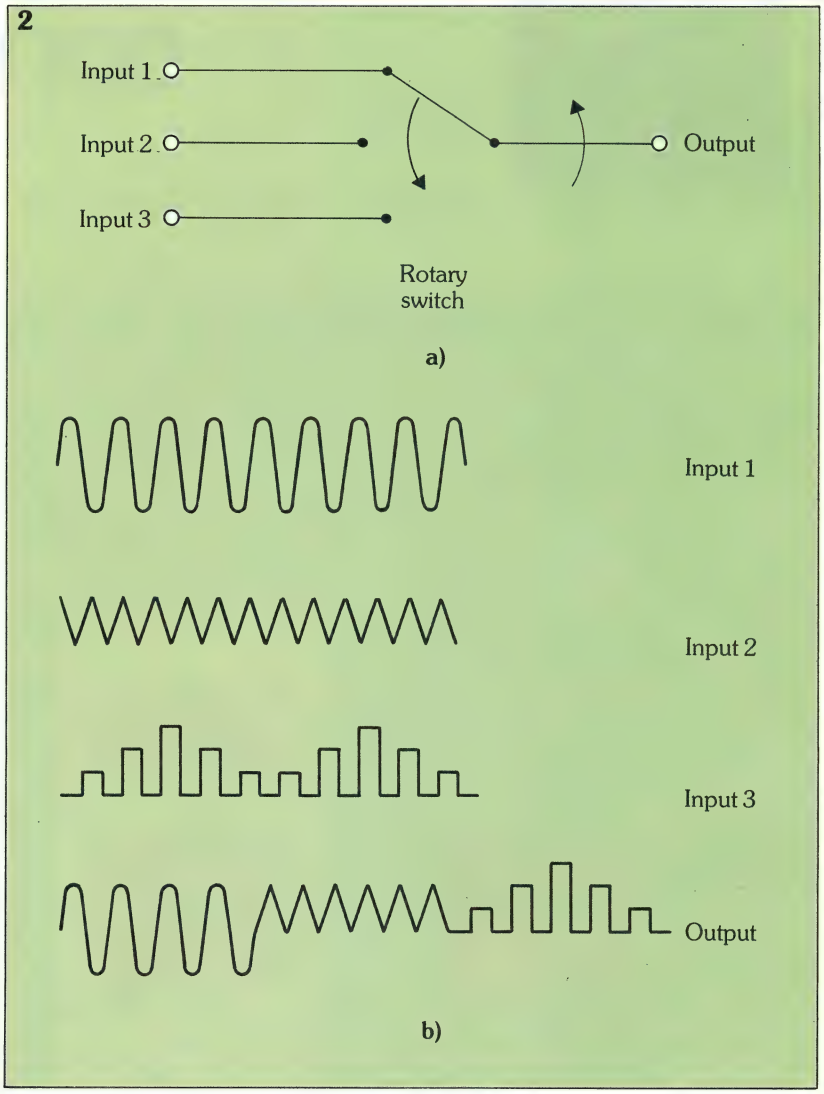
Analogue multiplexers

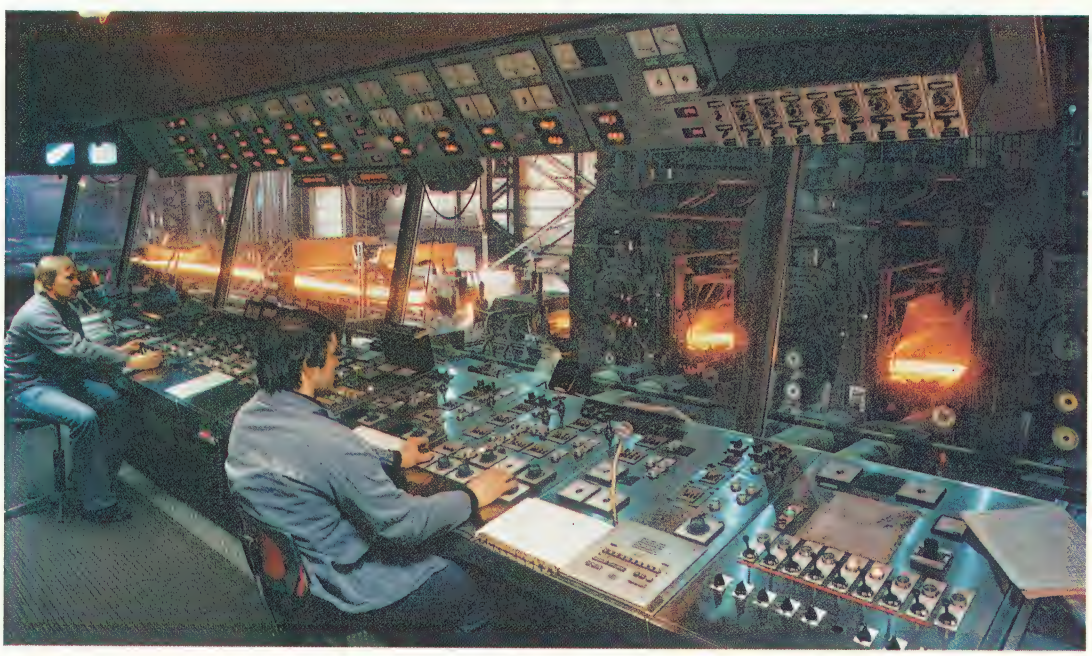
So far in our discussion we have been concerned with using ADCs to convert single analogue signals to digital codewords. However, in many applications a number of analogue signals may require conversion.

We have seen that typical ADCs are complex systems rather than simple circuits and are therefore quite costly. Obviously, in an application with many analogue input signals, the use of individual ADCs for each signal would be an expensive solution. Fortunately, in some cases, **analogue multiplexers** may be used which allow a single ADC to be *switched* between several analogue input signals. This switching between signals is an example of a common interfacing technique, which we shall look at in more detail in a later chapter, known as **time division multiplexing**.

Figure 2a shows the principle of time division multiplexing, where a mechanical rotary switch is switched between three input signals (a rotary switch is one which may be constantly turned in either direction so that the switch output is connected to each input in turn). The input and

2





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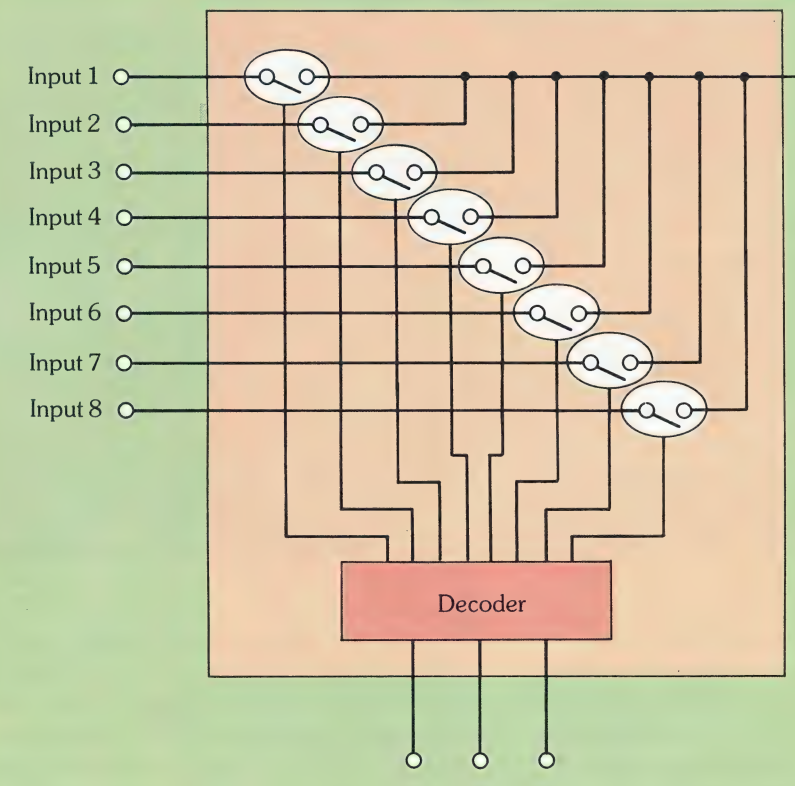
1. (a) How a sample-and-hold circuit and an ADC are connected; **(b)** timing diagram of the sampling pulse and the EOC signal.

2. (a) Time division multiplexing; (b) the input and output signals of the rotary switch.

Left: process control.

3. (a) Block diagram for an eight-input multiplexer; **(b)** truth table for this 3-bit to one-of-eight decoder.

3



a)

b)

3-bit input			Switch
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

output signals of the rotary switch are shown in *figure 2b* and we can see that the output is, in effect, a sample of each of the inputs in turn.

Of course, the switching mechanism in an electronic multiplexer must be capable of much higher speed switching than mechanical switches allow, and so electronic switches similar to types we have seen in earlier chapters are used in typical multiplexers. *Figure 3a* shows a block diagram of an eight-input multiplexer, which is represented by a bank of eight electronic switches and a decoder circuit. A 3-bit digital signal is decoded to switch on one of the eight electronic switches selecting the required input. A truth table for this 3-bit to one-of-eight decoder is shown in *figure 3b* and may be implemented with a logic circuit or a ROM-type device.

Typical multiplexers available use switches based on the circuit of *figure 4*. Two complementary MOSFETs are connected in parallel and their gates are connected via an inverter. Thus, when the gate of the n-channel MOSFET T_1 is at logic 1, the p-channel MOSFET T_2 is at logic 0. Both MOSFETs are on and present

a low drain-source resistance (in the region of only about 100 Ω) allowing the applied analogue input signal to pass to the output. However, when the MOSFET T_1 gate is logic 0, the gate of MOSFET T_2 is logic 1 and both MOSFETs are off.

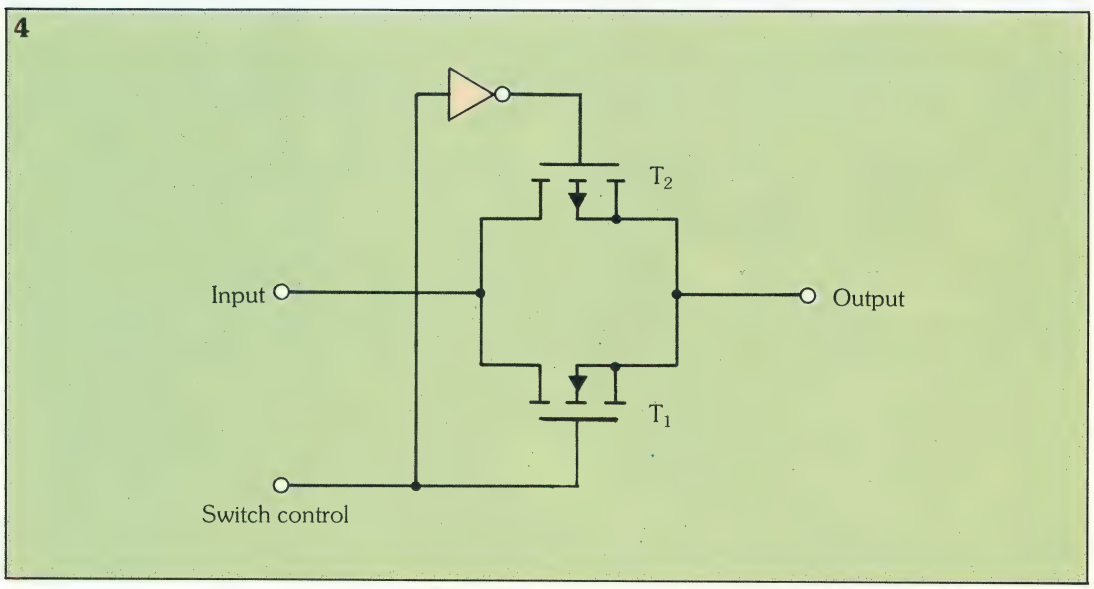
Extremely high drain-source resistances exist (in the order of MΩ) preventing passage of the input analogue signal. If you remember, we have seen similar devices to this switch, in our discussion on three-state outputs of digital circuits which connect to data busses – transmission gates. The operation and construction of these analogue multiplexer switches is similar to transmission gates; they are, in fact, the analogue analogue of digital transmission gates! For a more detailed description of their operation see *Digital Electronics 15*.

The multiplexer of *figure 3a* uses individual switches to select the required individual analogue input. We have assumed that the second input connection (i.e. each signal's ground) is common to all inputs and output. This type of multiplexer is known as a **single-ended multiplexer**. Another type, the **differential-input multiplexer**, can be manufactured, in which *pairs of switches* are operated, to connect *two* selected inputs to the multiplexer's *two* outputs. Differential-input multiplexers are useful if the following circuit's input is of the differential amplifier type, where the *difference* between the amplifiers's two inputs is amplified. *Solid State Electronics 24* describes this amplifier in detail.

Complete data conversion systems

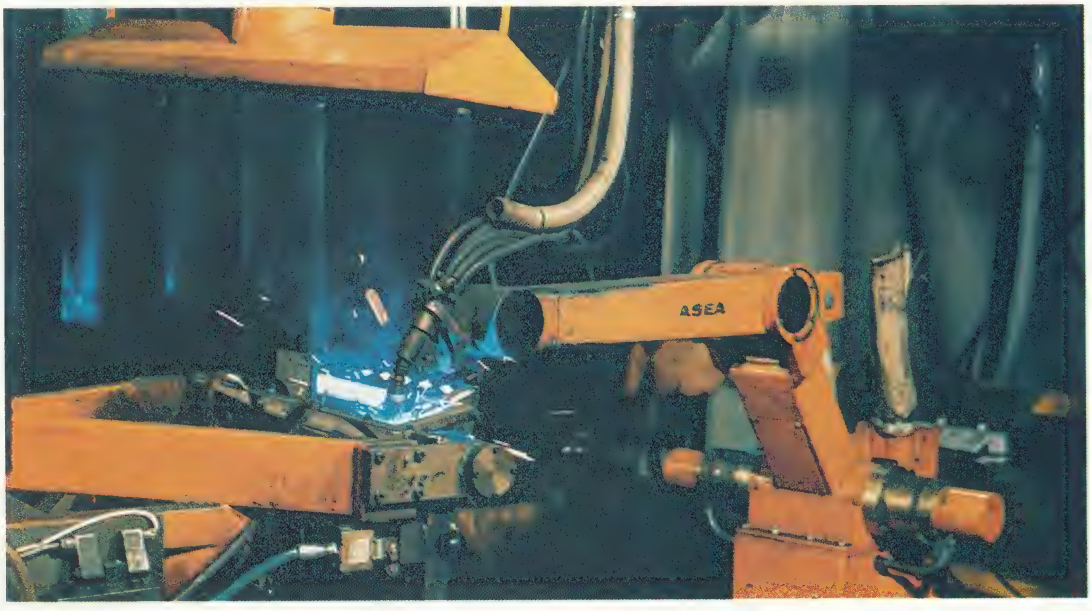
The analogue-to-digital and digital-to-analogue conversion systems we have seen are rarely used by themselves and normally form only part of a complete data conversion system. We may therefore be justified to think of ADCs ad DACs, together with their associated peripheral circuits such as filters, amplifiers, sample-and-hold etc., as *subsystems* of complete systems. In this respect, the subsystem operation is usually controlled by the system controller – often a computer or a microprocessor. A possible example of a conversion system is shown in *figure 5* where a multiplexer is used to combine analogue inputs corresponding to water temperature and steam pressure in a boiler. A single sample-and-hold samples each of the analogue inputs in turn and an ADC converts the samples to digital codewords which are presented to the bidirectional data bus. Also connected to the data bus are two DACs: one which provides an analogue output to control the boiler's heater coil; the other similarly controls the steam outlet valve. A computer is used which controls all operations within the system.

Water temperature is detected by a **thermocouple**, a device which, for our purposes, we can see to be a converter of temperature into voltage – the greater the



4. Typical multiplexers use switches based on this circuit.

Right: an arc welding robot. Both analogue-to-digital and digital-to-analogue conversion occurs during this process.



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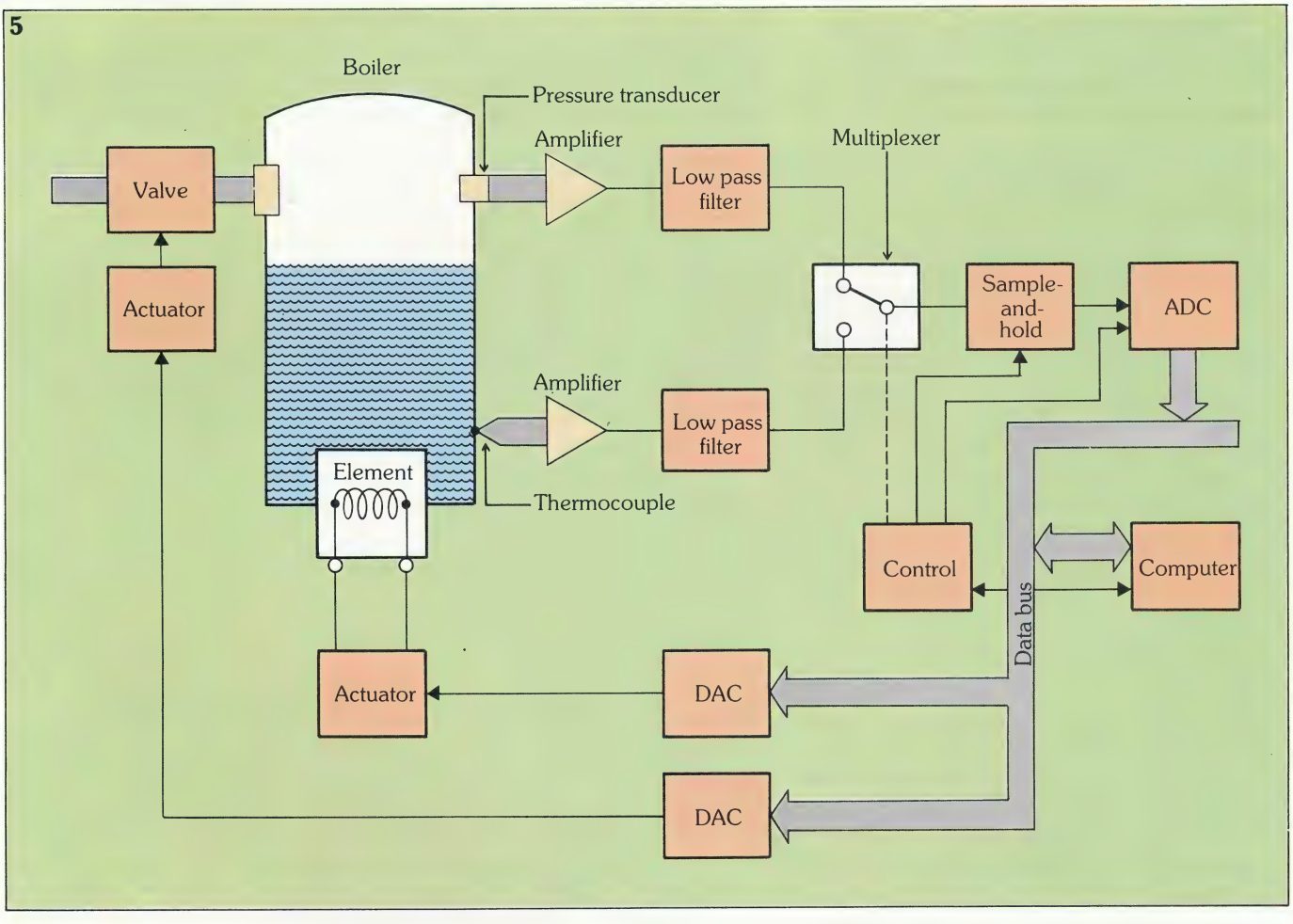
5. An example of a data conversion system.



temperature, the greater the voltage. A thermocouple is a form of **transducer**, i.e. it converts a measure of one form of energy into another form. A pressure transducer is similarly used in this example to detect the boiler's steam pressure, converting it, too, to voltage.

Transducers of many different types,

converting measures of many kinds of energy into others, are available. Another example of a temperature transducer is used in the second conversion system example shown in *figure 6*. Here, the possible circuit of an electronic thermometer with a digital display is shown, where the temperature transducer is a forward biased n-p-n transistor. Operating in this mode, the transistor has a temperature coefficient of 2 $mV°C^{-1}$, so a rise in temperature of say, 100 °C, causes a voltage change across the transistor of 200 mV. A reference voltage is applied to the collector of the transistor, holding it at a fixed voltage. The emitter voltage of the transistor – which therefore depends on ambient temperature – is detected by the ADC integrated circuit, the 14433. The ADC contains all analogue-to-digital and coding circuits to provide a BCD output. The BCD signals are then decoded by three 4543 latch/decoder/driver ICs for digital temperature display on an LCD.

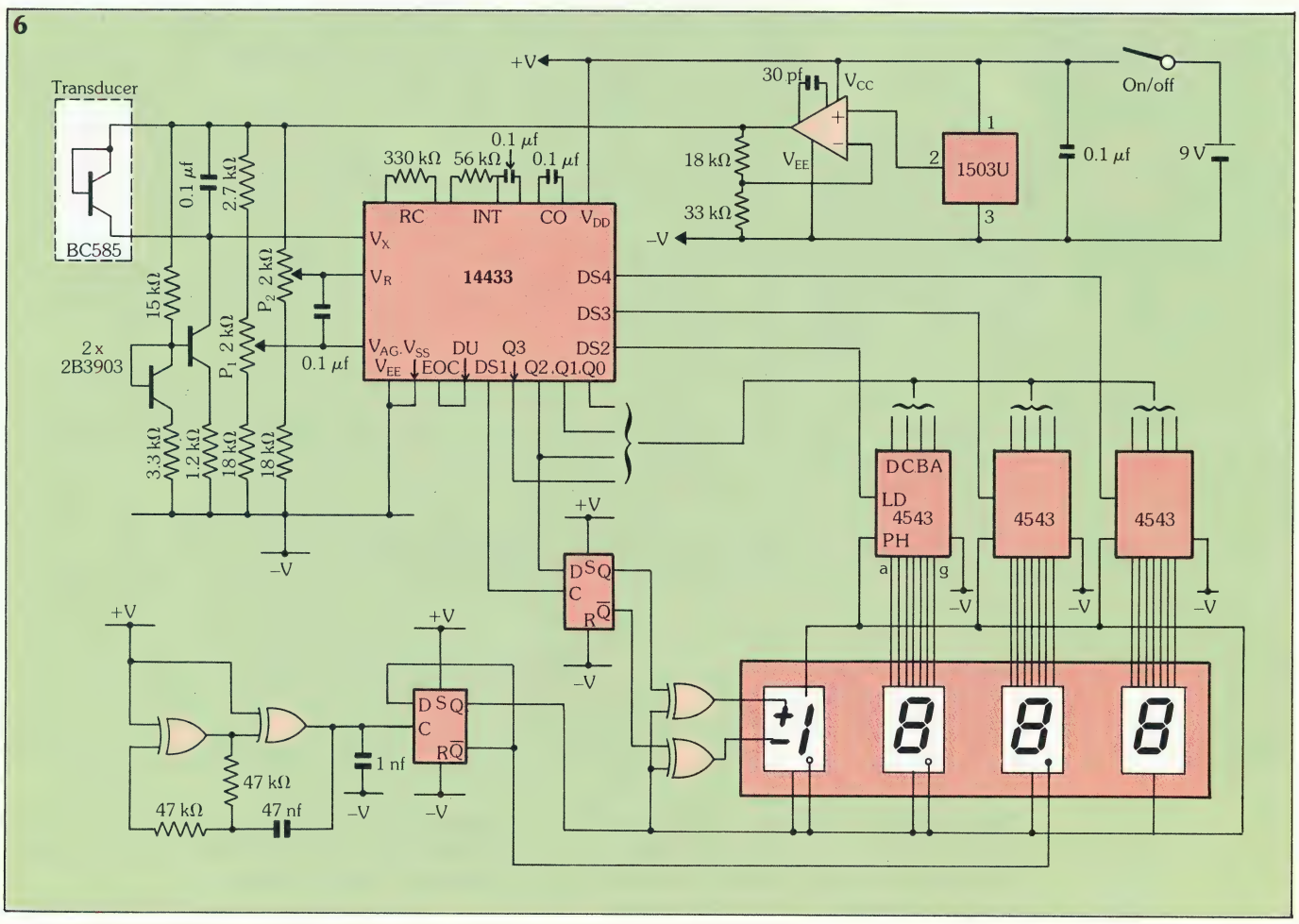
Accuracy of data conversion systems

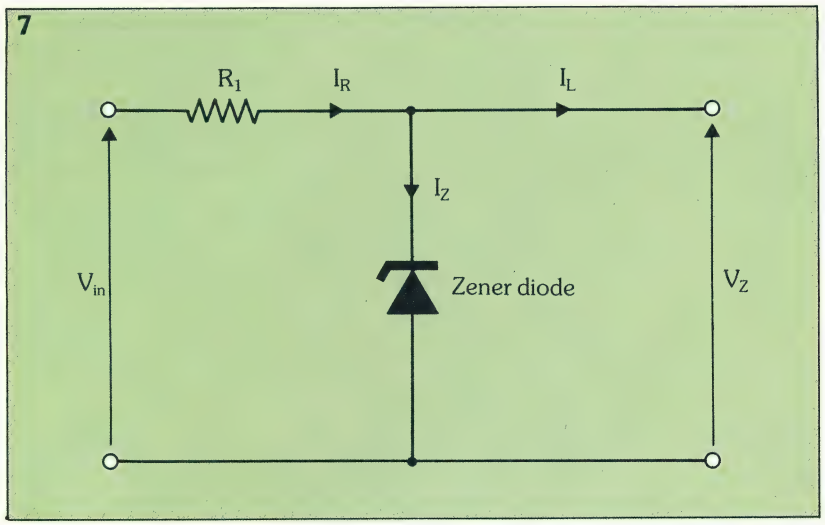
Analogue-to-digital and digital-to-analogue conversion subsystems are used because of the inherent high levels of accuracy of digital electronics. In any data conversion system, therefore, the accuracy of each digital subsystem must at least match that of the analogue system it replaces, otherwise there is little point in the application. System accuracy and its definition is thus an important subject when dealing with any analogue-to-digital or digital-to-analogue conversion. The important points concerning accuracy within a data conversion system are detailed below.

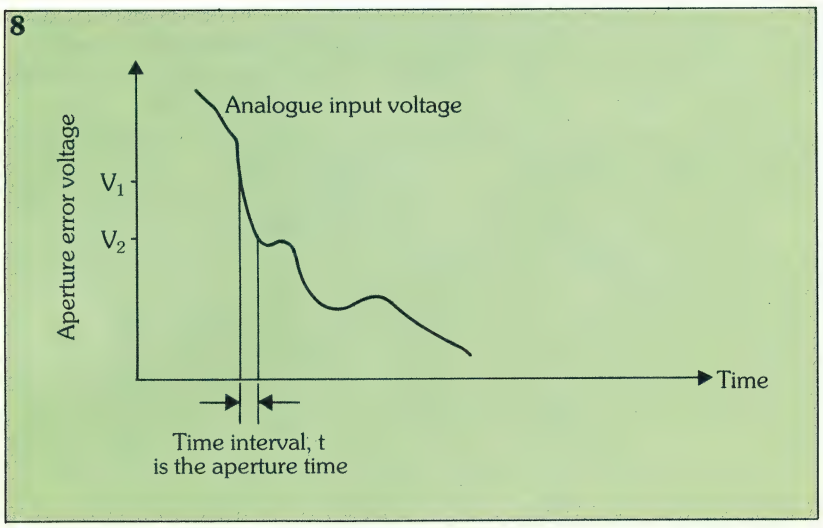
ADCs and DACs

Quantization error is the most fundamental parameter which affects accuracy. This quantization error is, however, directly related to the number of bits in the digital

6. A circuit for an electronic thermometer with a digital display.







7. A Zener diode is used to provide constant reference voltages.

8. Graph of a rapidly changing analogue voltage over a period of time, t, showing the aperture error voltage.

codewords used, and so by increasing the bit number we can decrease the quantization error, therefore increasing conversion accuracy. For example, the quantization error of a 4-bit ADC/DAC combination is one part in 15; the quantization error of a 5-bit combination is one part in 31; an 8-bit combination error is one part in 255.

The reference voltages used in ADCs and DACs can also affect overall system accuracy. Any small variations in reference voltages will inevitably affect performance if the converters rely on *constant* potentials. Many devices exist which may be used to provide constant reference voltages, the simplest of which is the Zener diode shown in *figure* 7. As we know, a Zener diode is reverse-biased in operation and exhibits a reverse breakdown at its fixed Zener voltage, V_z. For a given input voltage V_{in}, the voltage across the resistor R_1 is $V_{in} - V_z$. At this input voltage, the current through the resistor is:

$$I_R = \frac{V_{in} - V_z}{R_1}$$

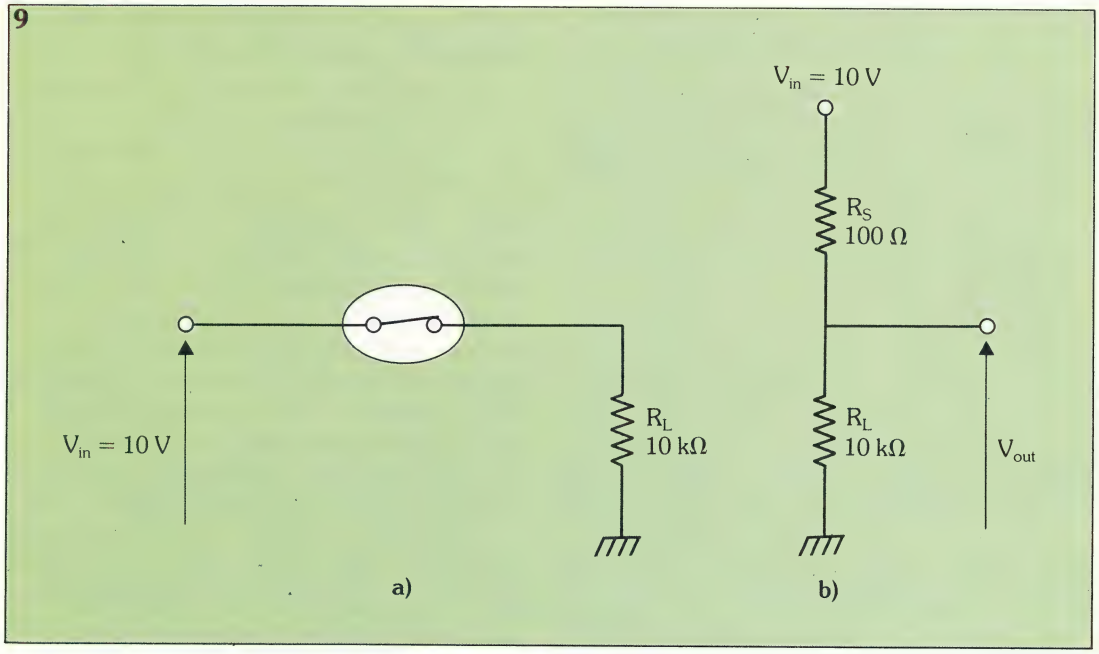
From Kirchhoff's laws we know that the sum of the two currents, I_L (through the load circuit) and I_z (through the Zener diode), equals current I_R, so a fall in load current causes an increase in current through the Zener diode. Similarly, an increase in load current causes a reduction of Zener diode current. The outcome of the circuit is thus to create a stable output voltage, regardless of output load current, within the circuit's operating limits.

Many other devices, generally based on this Zener breakdown effect, are available in integrated circuit form, and are capable of providing a stable reference voltage at currents up to many amps.

Sample-and-hold circuits

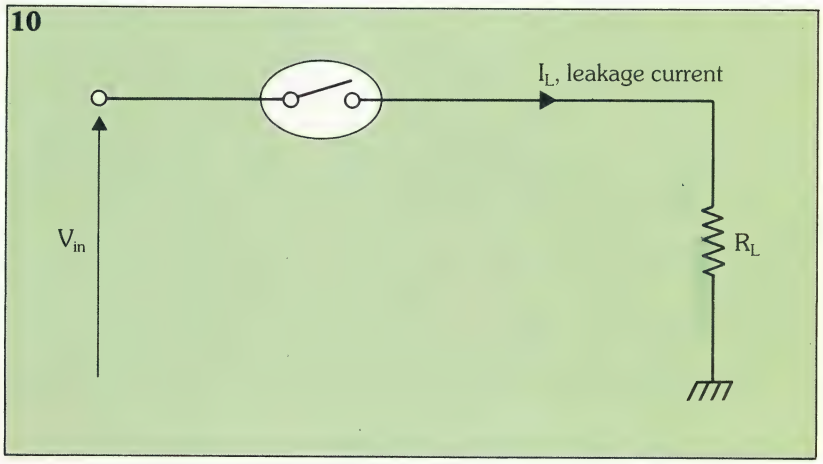
The circuits we have previously described which perform the sample-and-hold function can also introduce errors into the conversion process. Generally, three types of errors can be caused by a sample-and-hold circuit. The first is due to charge loss from the circuit's storage capacitor and is measured as a rate of change of output voltage from the sample-and-hold, known as the **droop rate**. Charge loss from the capacitor can be minimised with careful design and use of high input impedance amplifiers to buffer the capacitor output voltage. However, it cannot be eliminated because, inevitably, a small leakage current will always flow through the dielectric of the capacitor itself.

A second form of error caused by sample-and-hold circuits is inherent within their operation, and is an effect of the finite time it takes to switch a circuit from one sampling state to the next. *Figure 8* shows an example where a rapidly changing analogue voltage is sampled over an interval of time, t. At the beginning of this interval of time the voltage stored across the internal capacitor, i.e. the held voltage, is shown as voltage V_1. However, the voltage V_2, at the end of time t, is correspondingly lower because the analogue voltage has fallen. The delay in switching is known as a sample-and-hold



9. (a) An electronic switch in its 'on' state; **(b)** an equivalent circuit showing how voltage is lost across the on-resistance of the switch.

10. When the switch in *figure 9a* is off, leakage current, I_L, flows through the circuit.



circuit's **aperture time** and the error in voltage caused by the finite aperture time, $V_1 - V_2$ (in this example), is called the **aperture error voltage**.

Feedthrough of a sample-and-hold circuit, i.e. the fraction of the input signal appearing at the output, is a third form of error. The effects of feedthrough, although minimal at low frequencies, can be quite significant at high frequencies where parasitic capacitances within the circuit assume low impedances. A parasitic capacitance between drain and source of the sample-and-hold circuit's electronic switch, for example, will have a very high impedance at low frequencies and the circuit will function as we wish. At high frequencies, on the other hand, this parasitic capacitance will have a low impedance and so part of the analogue input signal will feed through to the output of the circuit – *whether the electronic switch is on or off.*

The electronic switches used in data conversion circuits can create further problems which may affect system accuracy. In our discussions of the uses of electronic switches in digital-to-analogue and analogue-to-digital conversion, and sample-and-hold circuits, we have assumed that the on and off states of the switches (corresponding to resistances of approximately 100 Ω and 10 MΩ) are ideal. In reality of course, this is not the case.

An electronic switch is seen in its on state in *figure 9a*, where an input voltage of 10 V is connected to a load resistance of 10 kΩ. The equivalent circuit of this circuit is shown in *figure 9b* and it is easy to see that the switch forms the upper arm of a potential divider. Using the potential divider formula, we may calculate the output of the circuit to be:

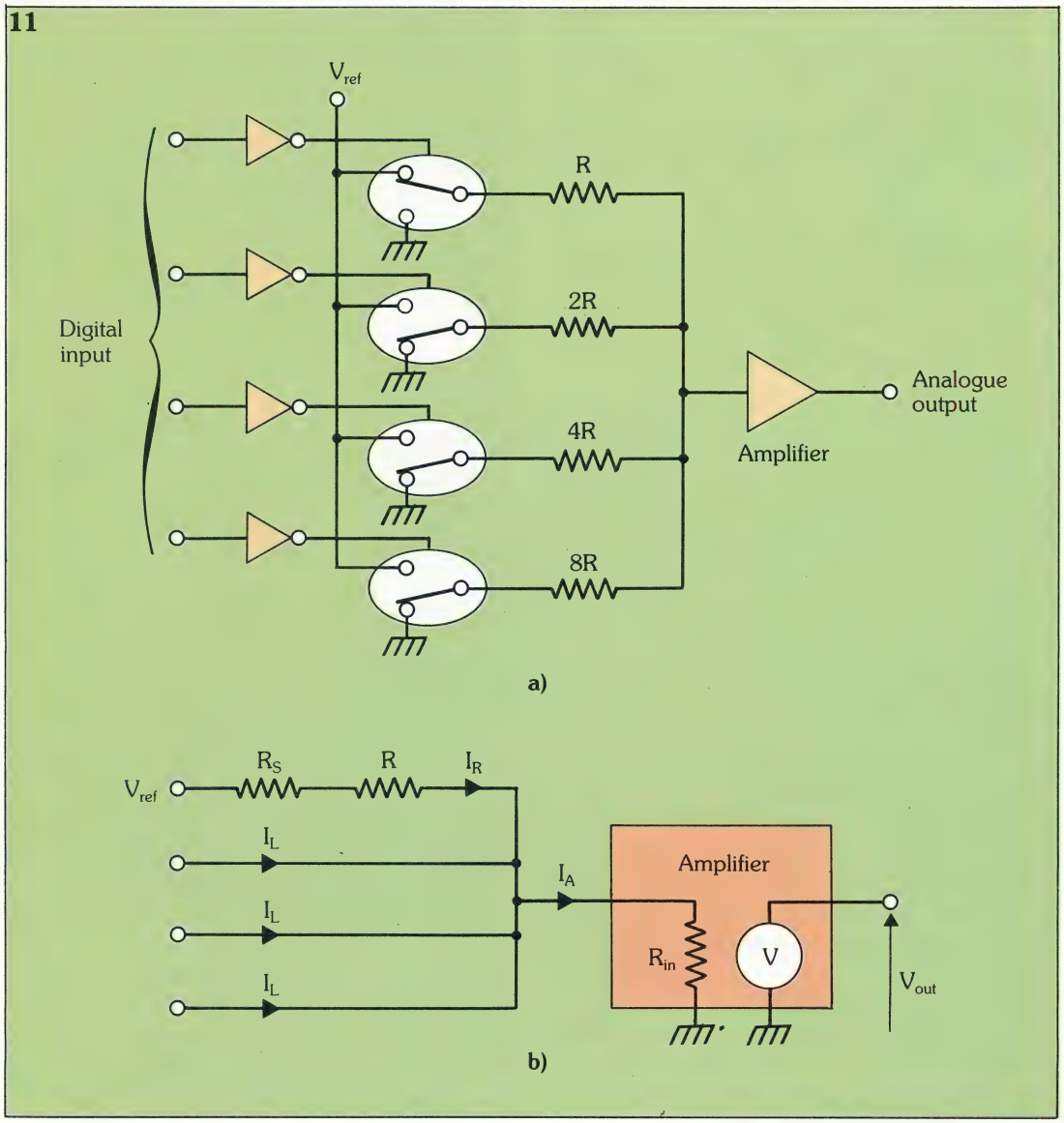
$$V_{out} = \frac{R_L}{R_L + R_s} V_{in}$$

$$= \frac{10\,k}{10k + 100} 10$$

$$= 9.9\,V$$

So, 0.1 V has been dropped or lost across the on-resistance of the electronic switch.

When the switch is off, the opposite effect occurs. Because the switch has a finite resistance, albeit very high, a small



11. (a) Binary weighted network and amplifier circuit with one switch on and three switches off; **(b)** equivalent circuit.

current will always flow, as in *figure 10*. This current I_L, is known as a leakage current.

We can see how these effects of switch on-resistance and leakage current can affect the accuracy of data conversion circuits if we take a couple of examples. In the first example we shall look back to the circuit of a binary weighted resistor network, which used a reference voltage and electronic switches. The circuit, from *Digital Electronics 19*, is reproduced in *figure 11a*, but is shown with one switch on, and three switches off. We can consider the output voltage of the circuit to be the input voltage to the amplifier multiplied by the amplifier gain, 2. This is a very simple description of amplifier output voltage but one which will do for our purposes here. *Figure 11b* shows an equivalent circuit of this binary weighted network and amplifier, and we can see that the amplifier input voltage is generated by a current flowing through an input resistance.

The input current to the amplifier, I_A, is a sum of the current through resistor R and the leakage currents through resistors 2R, 4R and 8R. The current through resistor R may be calculated, using Ohm's law, by:

$$I_R = \frac{V_{ref}}{R + R_s}$$

The currents through each of resistors 2R, 4R and 8R are simply the leakage currents of the switches, so the total amplifier input current is:

$$I_A = I_R + 3I_L$$
$$= \frac{V_{ref}}{R + R_s} + 3I_L$$

and the amplifier input voltage is thus:

$$V_{in} = I_A R_{in}$$
$$= \left(\frac{V_{ref}}{R + R_s} + 3I_L\right) R_{in}$$

If $R = 10\,k\Omega$, $R_s = 100\,\Omega$, $V_{ref} = 10\,V$, $I_L = 10\,nA$ and $R_{in} = 10\,k\Omega$, then:

$$V_{in} = 9.9\,V$$

and, as the amplifier gain is 2, the circuit output voltage:

$$V_{out} = 19.8\,V$$

If 'perfect' switches were used with 0 Ω on-resistances and 0 nA leakage currents, the output voltage can be calculated to be 20 V. So, the error in output voltage introduced by the non-perfect electronic switches is 0.2 V, or 1% of the ideal.

We can reduce the effect of switch on-resistance by increasing the input resistance of the amplifier and the resistor values in the binary weighted network. If, say, in the above formula for amplifier input voltage, $R = 1\,M\Omega$ and $R_{in} = 1\,M\Omega$, the amplifier input voltage:

$$V_{in} = 10.03\,V$$

and so the amplifier output voltage:

$$V_{out} = 20.06\,V$$

So, although the on-resistance error has been reduced, the error due to leakage current has *increased*.

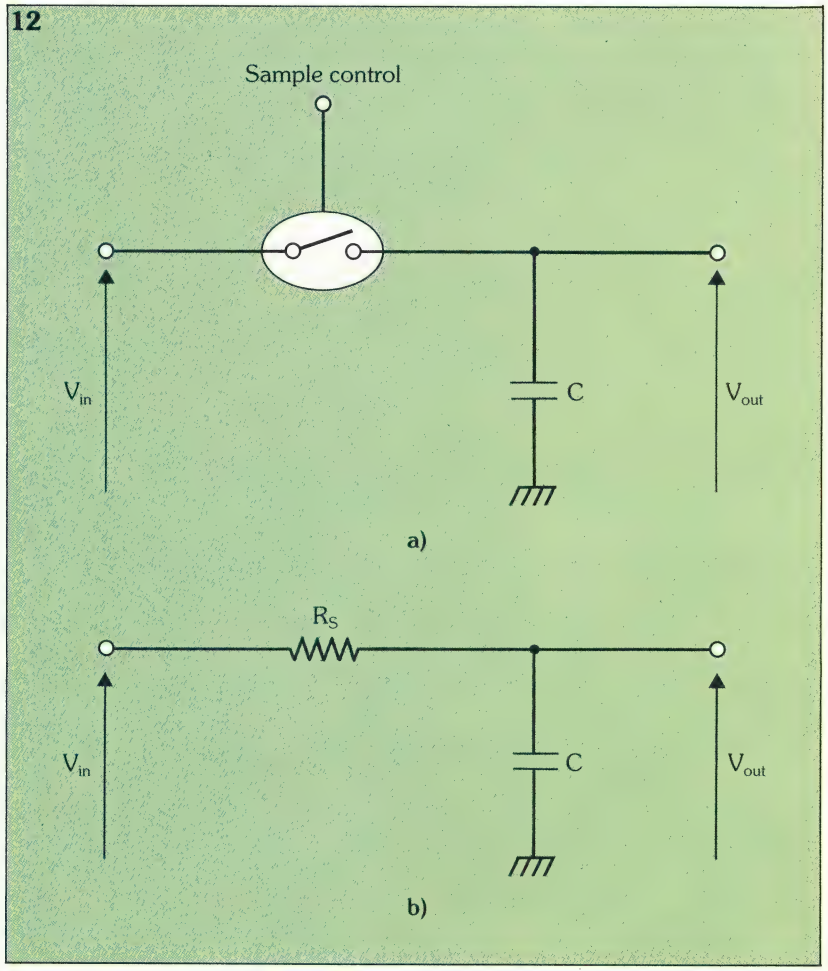
Leakage current through the electronic switches of a multi-input device such as a multiplexer manifests itself as a phenomenon known as **cross-talk**. The name cross-talk arises from the same effect which occurs in telephone systems, where other conversations are heard faintly in the background of an existing conversation link. Electronic switch leakage currents, and hence multiplexer cross-talk, increase with frequency due to the parasitic capacitances between drain and source of the FET-type switches.

A second example of how non-ideal electronic switches can affect system accuracy can be seen in their use in sample-and-hold circuits. A simple sample-and-hold circuit is shown in *figure 12*. Ideally, when the sample-and-hold circuit is required to sample input voltage V_{in}, the electronic switch is closed and the capacitor instantly charges up to the applied voltage. However, the presence of the switch on-resistance prevents this instant charge up, creating a time constant equal to R_sC. The voltage across the capacitor thus charges up exponentially with this time constant, and takes a finite time to **settle** to its final value. The sample-and-hold **settling time** is calculated as a specified number of time constants, typically nine time constants, which is the time the capacitor voltage takes to settle to within 0.01% of its final value.

Finally, we will now take a look at the effects of the other peripheral circuits, i.e. amplifiers and filters, used in data conversion systems. We have just seen how an amplifier's input resistance can affect the accuracy of a DAC or a multiplexer, and as these circuits are used within ADCs, the whole system is therefore affected.

The frequency components which a filter allows to pass or filters out are often of critical importance; obviously, as much of the original signal as possible is preferred

12



12. (a) Sample-and-hold circuit; (b) equivalent circuit.

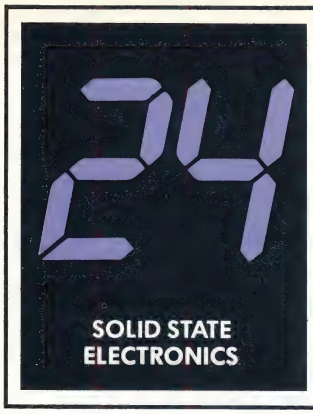
when sampling before analogue-to-digital conversion, but if frequency components of too high a frequency are sampled, low frequency aliases will be generated on digital-to-analogue reconversion.

Amplifier gain can play an important part in reducing quantization errors. Take, for example, an 8-bit ADC which will have a minimum quantization error of one part in 255, or 0.4%. If the input voltage range to this ADC is, say, 20 V, but the applied analogue signal has a range of only 2V, then only one tenth of the possible range of digital output codewords are used and the quantization error will be 4%. An amplifier with a gain of 10 should be used to increase the applied input analogue signal range to match the range of the ADC input.

On the other hand, if the input analogue signal range is larger than the ADC input range, distortion will occur. Such larger input signals must first be attenuated or reduced before conversion.

Glossary

analogue multiplexer	device which can be switched between a number of analogue input signals. A multiplexer's output signal is thus dependent on the chosen input signal
aperture time	the delay in switching of a sample-and-hold circuit's electronic switches. The aperture time causes an aperture error voltage at the circuit's output
cross-talk	errors in the output signal of a multiplexer, or similar device, where unwanted signals are present. In a multiplexer, leakage currents of electronic switches which are off introduce cross-talk
differential-input multiplexer	multiplexer in which the electronic switches are grouped in pairs. Used when connecting pairs of analogue signals to differential amplifiers
droop rate	rate of discharge of the capacitor of a sample-and-hold circuit, producing a falling voltage at the circuit's output
end of conversion (EOC)	signal sent to a sample-and-hold circuit requesting a new sample to be taken
feedthrough	fraction of the analogue input signal of a sample-and-hold circuit appearing at the output of the circuit. Caused by parasitic capacitances. The effect increases with frequency
leakage current	current through an electronic switch when off
on-resistance	finite resistance of an electronic switch when on
time division multiplexing	technique in which many input signals are sampled and combined together as one composite output signal
settling time	time taken by a sample-and-hold circuit for the output voltage to be within a specified percentage of its final value, typically within 0.01%
single-ended multiplexer	multiplexer whose inputs and output signals share a common ground
thermocouple	transducer which may be used to measure temperature
transducer	device which converts a measure of one form of energy into another



Operational amplifiers

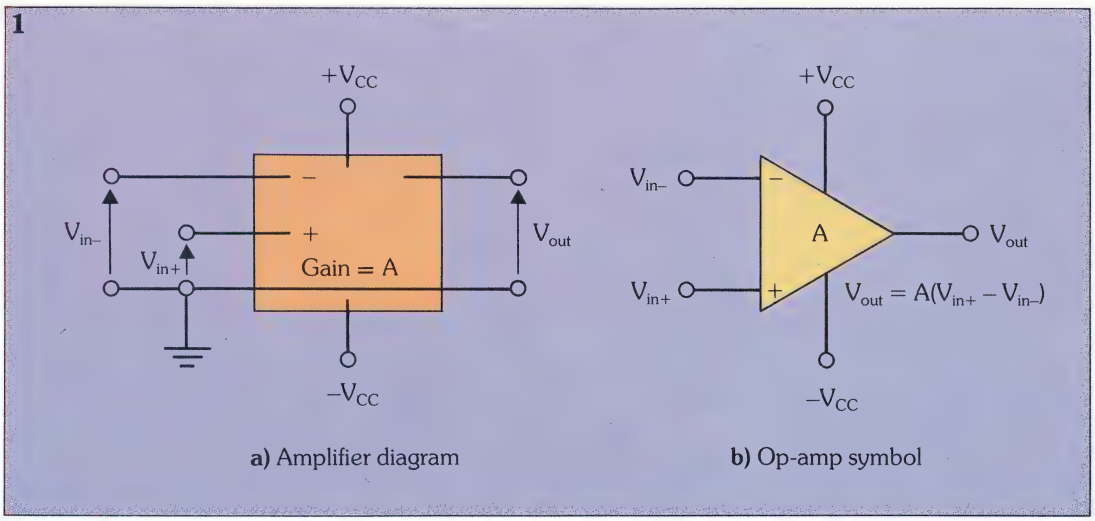
What are op-amps

Operational amplifiers (commonly abbreviated to op-amps) are linear circuits that were originally designed to perform mathematical operations in analogue computers. Op-amps were initially manufactured from discrete components, however, the development of integration techniques now means that these circuits are ready for operation with the addition of only a few discrete components.

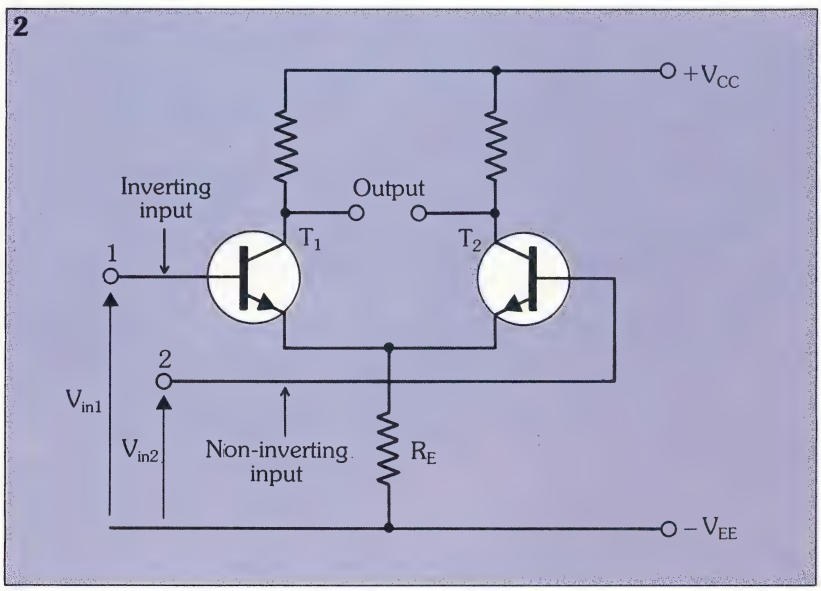
Op-amps can be used with different types of feedback and external circuitry to construct analogue computing circuits, such as summers and integrators, and also to make audio amplifiers, modulators, frequency dividers etc. Op-amps and digital circuitry in combination are widely used in instrumentation and control circuitry.

The term linear expresses the *regulatory* action of these devices, as opposed to the *switching* action of their digital counterparts. Since these linear ICs are amplifiers, their function is to increase the power, current or voltage that is applied to their inputs.

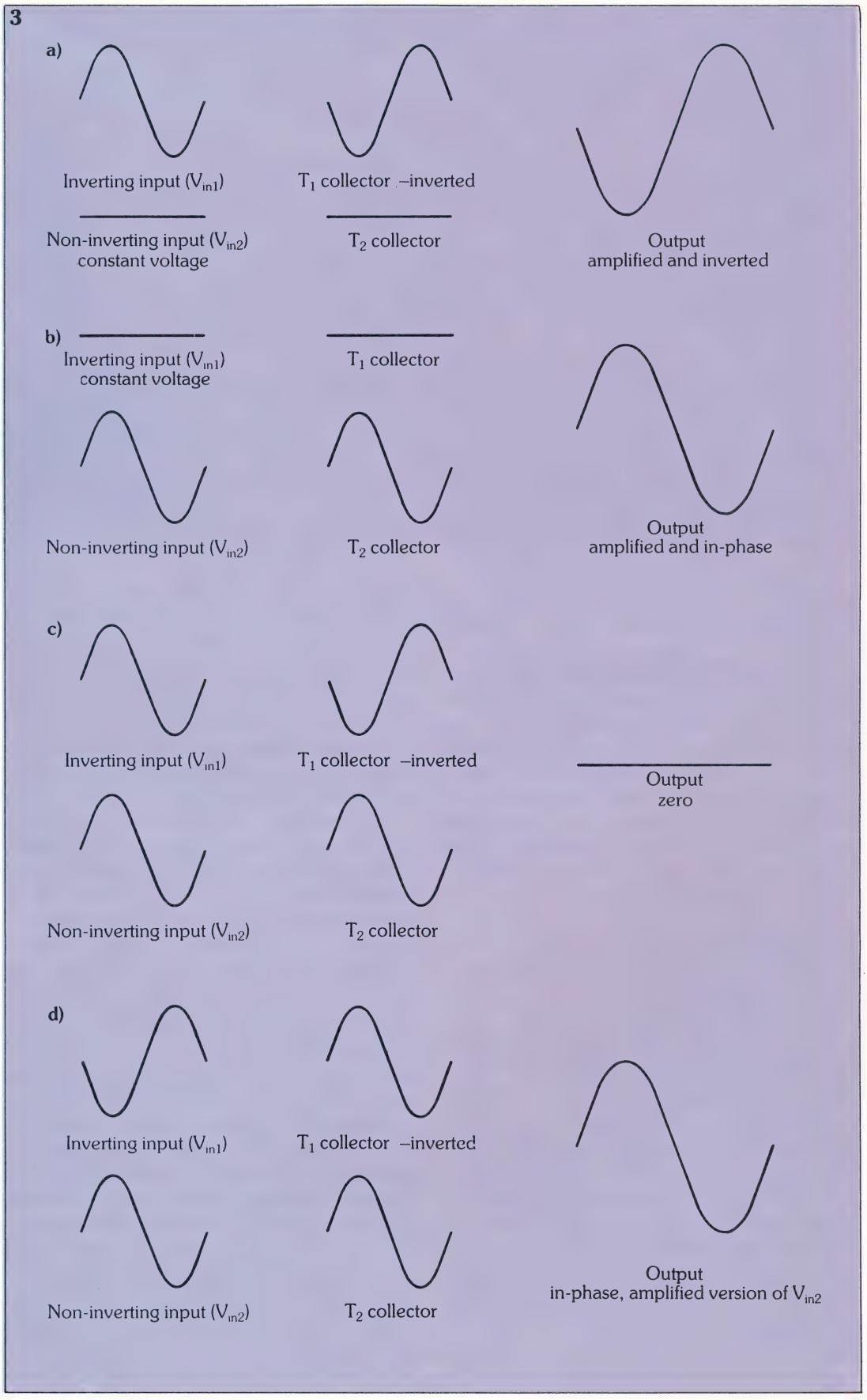
Figure 1 shows an amplifier diagram, and the corresponding op-amp symbol. As you can see, the op-amp has a negative and a positive input terminal (inverting and non-inverting) indicating that this is a **differential amplifier**. The output of the amplifier in *figure 1a* is therefore A (the gain) times $V_{in+} - V_{in-}$: the *difference* between the voltages at the non-inverting and the inverting input terminals. With the conventional symbol in *figure 1b*, it is understood that all the voltages are mea-



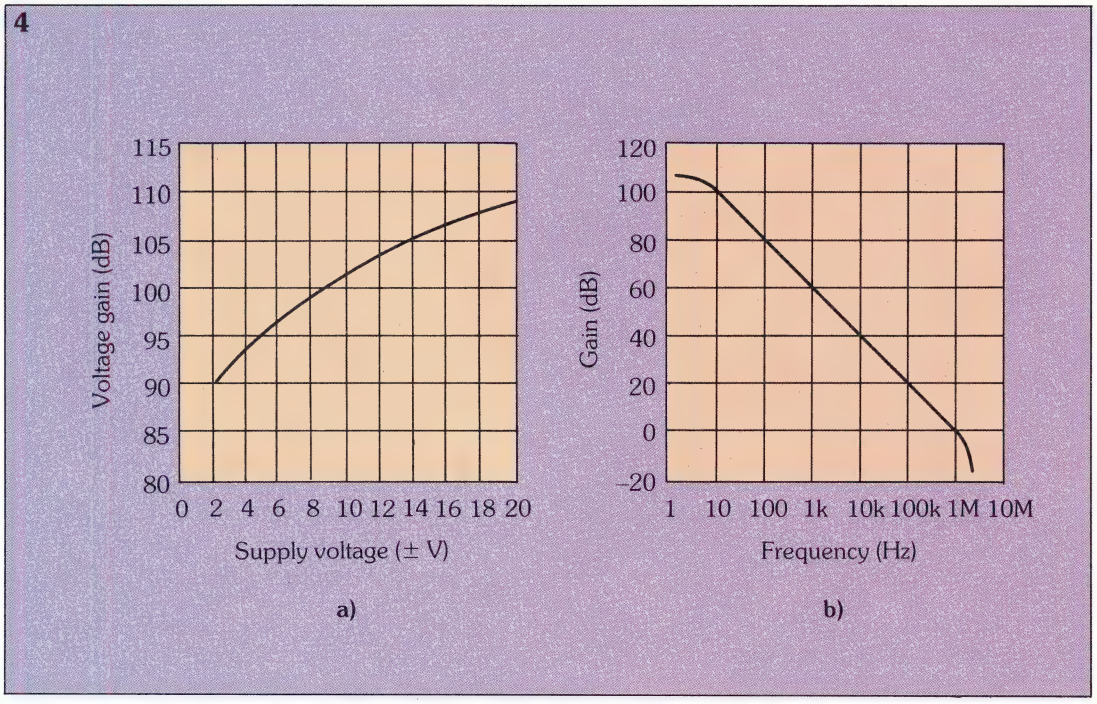
1. (a) Amplifier diagram; (b) op-amp symbol.



2. A differential amplifier circuit made from transistors connected in a longtailed pair.



3. Possible waveforms at selected points in the circuit of *figure 2*.



4. (a) Open loop gain as a function of supply voltage; **(b)** open loop gain as a function of frequency.

sured with respect to ground, so the input and output ground terminals are not shown.

A basic differential amplifier circuit made from bipolar transistors connected in what is known as a **longtailed pair** is illustrated in *figure 2*. This circuit could be used as a single input amplifier if the base of one transistor is connected to ground through resistance, but it is most commonly employed as a differential amplifier. One advantage of this type of circuit is that it is very stable if either the temperature or the supply voltage fluctuates. As both transistors will be identically affected, there will be no variation in output measured between the two collectors.

If voltage V_{in2} is held at a fixed voltage to correctly bias transistor T_2, and a signal (V_{in1}) is applied to the base of transistor T_1, then an increase in voltage V_{in1} will cause the collector current of transistor T_1 to rise and its collector voltage (V_{out1}) to fall. A rise in the current flowing through transistor T_1 increases the voltage across resistor R_E, thus reducing the bias voltage of transistor T_2. This, in turn, causes the collector current in transistor T_2 to fall and the collector voltage to rise. Output voltage V_{out2} can therefore be seen to be 180° out of phase with voltage V_{out1}.

Ideally, the current through resistor R_E is constant, which means that any increase or decrease in the collector current of transistor T_1 causes a corresponding decrease or increase in the collector current of transistor T_2. At worst, any current change through resistor R_E should only cause voltage changes across R_E of no more than a few tens of millivolts, and may be regarded as negligible.

If the circuit is used as a differential amplifier, then the two input signals have to be out of phase. While the input at one terminal rises, the input at the other terminal falls. The outcome, is that the output voltages will be 180° out of phase, and the voltage between the two collectors has twice the magnitude of the voltage at one collector. If the input signals are in phase (what are known as **common-mode signals**), then the output voltage at each collector will either rise or fall simultaneously. The output voltage across the two collectors will then be zero. Remember, this is a differential amplifier, and as there was no difference between the two input signals, then the combined output is zero.

To summarise the operation of this circuit, we can see that if input voltage V_{in2} is held constant, then a rise in voltage V_{in1} will bring about a rise in the collector current of transistor T_1 and a fall in the

collector current of transistor T_2, and vice versa. The final output voltage across the collectors will be an amplified version of the input signal (V_{in1}) but 180° out of phase. The V_{in1} input terminal is therefore called the **inverting input**.

If the signal had been applied to the V_{in2} input terminal while voltage V_{in1} was held constant, then the amplification would be the same as before, but the output would have been in phase with the input. The V_{in2} input terminal is therefore called the **non-inverting input**. If an identical signal is applied to both inputs simultaneously (common-mode signals) then the output will be zero. If the signals applied to the inputs are 180° out of phase however, then the difference between them will be amplified. This allows gains as high as 200,000 – known as **open-loop gains** in operational amplifiers. *Figure 3* summarises these conditions.

Open-loop gain

The open loop gain of an amplifier is the natural gain of the circuit – without any feedback applied to it – and is the ratio of voltage, V_{out}, to voltage, V_{in}. The 741 is an example of a commonly used integrated op-amp and this device has an open-loop gain of 200,000. This means that if a voltage of 50 μV is applied to the circuit's input, then the output is 200,000 times larger, i.e. 10 V.

The graph in *figure 4a* illustrates the nature of the open-loop gain of the 741 as it changes with the supply voltage; *figure 4b* shows how the open loop gain changes in relation to the frequency of the input voltage. As you can see, the gain in decibels becomes negative for frequencies above 1 MHz, in other words, the output is smaller than the input.

The **bandwidth** of an amplifier is the term given for the frequency range over which the gain does not fall by more than 3 dB. We can think of 'a fall of 3 dB' as meaning 'half power'. We will look more closely at dBs and their use later on. *Figure 4b* shows us that the **open-loop bandwidth** of the 741 is from 0 Hz (DC) to about 5 Hz. As you may guess, this is not a particularly useful figure, however, the bandwidth can be improved, at the expense of gain, by employing **feedback**.

Feedback

The two types of feedback, negative and positive, are employed for many different purposes in electronics. *Figure 5a* shows an op-amp in a **negative feedback** mode, while *figure 5b* shows it set up for **positive feedback**. The principle behind feedback, as you may remember from previous articles, is that part of the amplifier's output is diverted back to its inputs: if this is fed to the inverting input, then negative feedback results; if the non-inverting input is used, then positive feedback is created.

Using negative feedback, the op-amp's bandwidth can be improved as we have said, at the expense of gain. The basic arrangement of the circuit in *figure 6* shows how this can be done. As you can see, negative feedback is created by using a **closed loop** from the output to the inverting input, via the resistor R_f.

We have previously defined the amplifier's gain as being equal to the ratio V_{out}/V_{in}. In the case of an **open-loop amplifier** (one with no feedback), the gain is given the symbol A_{OL}. In the case of the **closed loop amplifier** (one with feedback) we use the symbol G. As you can imagine, the feedback is proportional to the output voltage (since it is derived from it), so, if we know what fraction the feedback is of the output voltage (termed β) we can work out the amplifier's gain.

The input voltage, V, to the differential op-amp shown in *figure 6* will be $V_{in} - \beta V_{out}$. Because $V_{out} = A_{OL} V$, then:

$$V_{out} = A_{OL} (V_{in} - \beta V_{out})$$

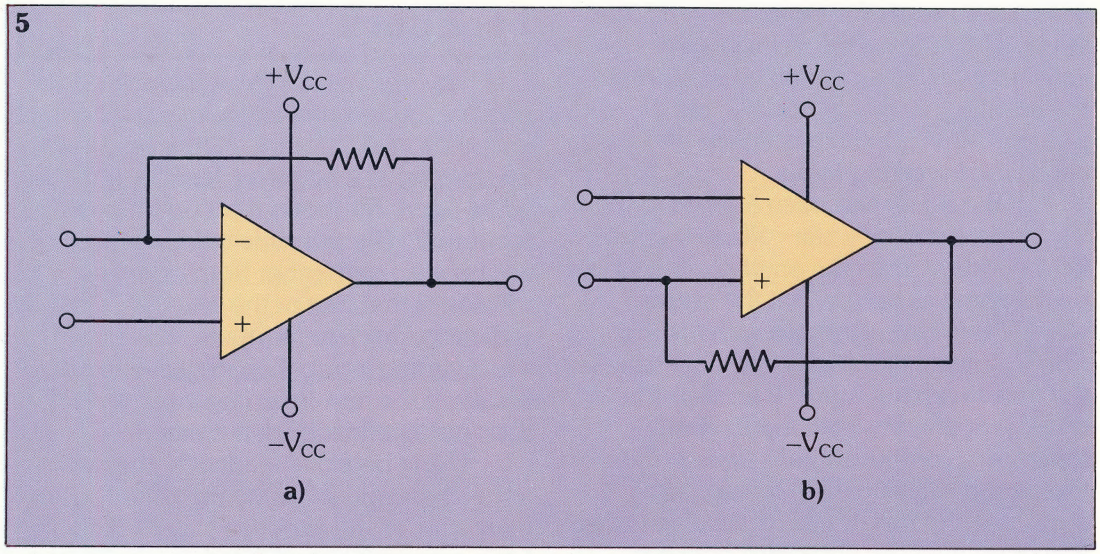
separating out V_{out} and V_{in} gives:

$$V_{out} (1 + \beta A_{OL}) = A_{OL} V$$

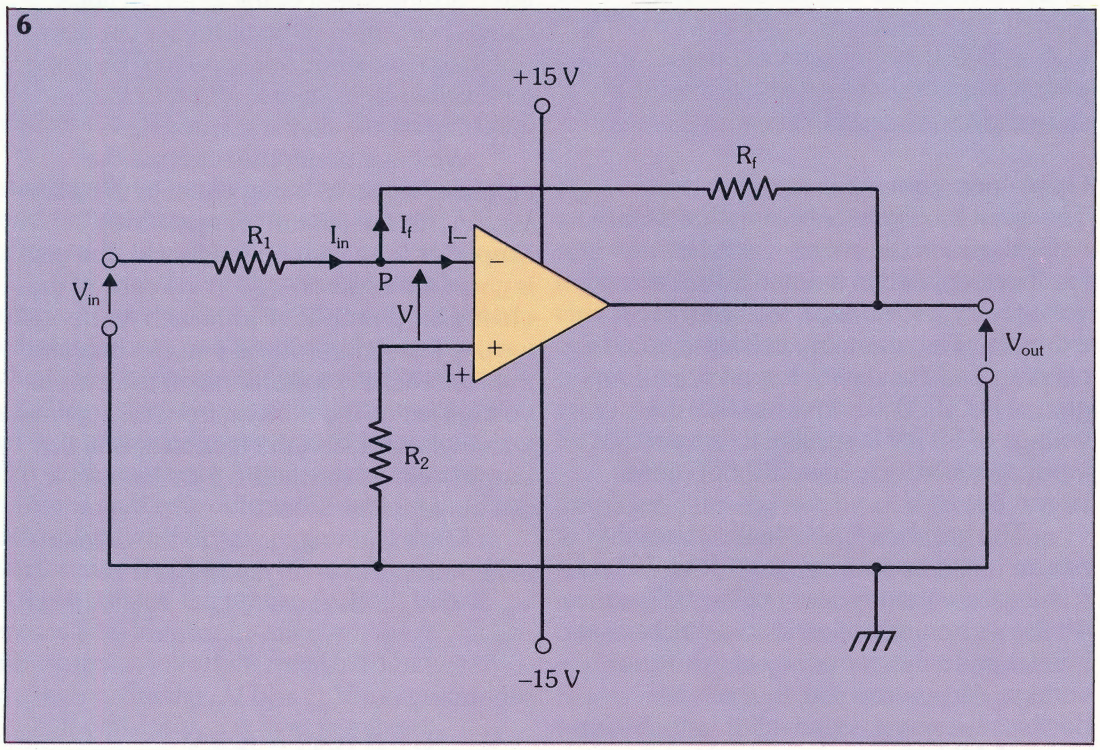
V_{out}/V, the effective gain of the circuit with negative feedback, is given by:

$$G = \frac{V_{out}}{V_{in}} = \frac{A_{OL}}{1 + \beta A_{OL}}$$

You can see that if there is no feedback, β will be equal to 0, and the gain will be equal to A_{OL}. The last equation shows that the gain with feedback (G) is equal to the gain without feedback (A_{OL}) divided by the term ($1 + A_{OL}$) which is known as the



5. An op-amp in negative feedback mode, (a) and positive feedback mode, **(b).**



6. Improving the op-amp's bandwidth at the expense of gain using negative feedback.

return difference, sometimes called the **feedback factor**.

We are not always concerned with exact quantities, providing close approximations can be made, simpler expressions will often suffice. The above equation can be simplified if we remember that an op-amp's open loop gain, A_{OL}, is very large – and so the term βA_{OL} may be large (depending on β). In such a case:

$$G = \frac{A_{OL}}{\beta A_{OL}} = \frac{1}{\beta}$$

The gain, therefore, depends on β if βA_{OL} is large enough.

As we said, β is a fraction of the output voltage and this fraction is determined by the ratio of the feedback resistor, R_f, to the input resistor, R_1. The gain, G, is therefore given by:

$$G = \frac{-R_f}{R_1}$$

This can be proved by examining the currents flowing in the circuit.

(continued in part 24)

TEST YOUR PROGRESS with the

I.T.E.C. QUIZ

DIGITAL ELECTRONICS – 20

1. The output of a comparator is:

a Logic 0 when either input is higher than the other
b Logic 1 when either input is higher than the other
c Logic 2 when either input is higher than the other
d Logic 0 or logic 1
e There is insufficient information to say

2. A follower converter uses one comparator for every quantization interval.

True or False?

3. The main difference between a successive approximation converter and a counter-ramp converter is:

a A counter-ramp converter uses a DAC
b A successive approximation converter uses a DAC
c A successive approximation converter uses a register
d a and c
e None of the above

4. In a flash converter:

a There must be one reference voltage for each quantization interval
b There must be seven comparators
c There must be eight resistors
d All of the above
e None of the above

5. All DACs require a sample-and-hold circuit in all applications.

True or False?

6. If an analogue signal, which is a sine wave of frequency 10 kHz, is sampled at a rate of 30 kHz:

a A low frequency alias of 30 kHz/10 kHz = 3 Hz will occur
b A low frequency alias of 30 kHz – 10 kHz = 20 kHz will occur
c A low frequency alias of a random frequency will occur
d All of the above
e None of the above

DIGITAL ELECTRONICS – 21

1. A single-ended multiplexer is one in which:

a There is only one input
b There is only one output
c All inputs and outputs are connected
d All inputs and outputs share a common ground
e None of these

2. A transducer is a device which may be used to convert all the energy generated in one form into another form of energy.

True or False?

3. Data conversion systems, in which analogue signals are converted to digital codewords and/or vice versa, are always more accurate than their analogue system counterparts.

True or False?

4. Question 3 is true, because:

a Digital circuits are inherently more accurate than analogue circuits
b Analogue signals are only an approximation of the real digital codewords
c Digital codewords of many bits may be used
d Question 3 is not true

5. Feedthrough of a sample-and-hold circuit is:

a Dependent on the storage capacitor
b Dependent on the input signal's frequency
c Dependent on the electronic switch
d a and b
e a and c
f b and c
g All of these

6. What is the settling time to within 0.01% of a sample-and-hold circuit with a storage capacitor of value 1 μF and an electronic switch with on-resistance 150 Ω.

a 1.35×10^{-3} s
b 1×10^{-4} s
c 0.74×10^{3} s
d All of these
e Not enough information is supplied
f None of these

7. The quantization error of a 6-bit ADC with an input range of 10 V, when an analogue input signal of 6 V range is applied is:

a 3.2%
b 2.6%
c 2.2%
d 1.9%
e 1.5%
f 1.2%

Answers to last week's quiz

BASIC COMPUTER SCIENCE – 14
1 e
2 a
3 d
4 c

DIGITAL ELECTRONICS – 19
1 a
2 e
3 a
4 d
5 b
6 c

SOLID STATE ELECTRONICS – 23
1 True
2 False
3 f
4 b
5 True
6 c
7 True

COMING IN PART 24

Solid State Electronics 24 continues with a discussion of **frequency dependent feedback, positive feedback** and **non-inverting** and **summing amplifiers.**

Digital Electronics 22 is the first of two articles concerning **instrumentation** and **control systems.**

Computers in Society I begins the series with a look at how the **new technologies have affected the home**, and speculates a little on what one might expect to see in the future.

Solid State Electronics 25 continues our discussion of operational amplifiers.

PLUS: *Basic Theory Refresher:* looking at **real** and **reactive power**.